Welcome To

ISSCC 2014
SESSION 9
Low-Power Wireless

A Self-Calibrating NFC SoC with a Triple-Mode Reconfigurable PLL and a Single-Path PICC-PCD Receiver in 0.11μm CMOS

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Outline

- Background
- Challenges
- Proposed Solution
  - Synthesizer Architecture
  - Receiver Architecture
  - Polling and Calibration Schemes
- Measurement Results
- Conclusion

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- **Background**
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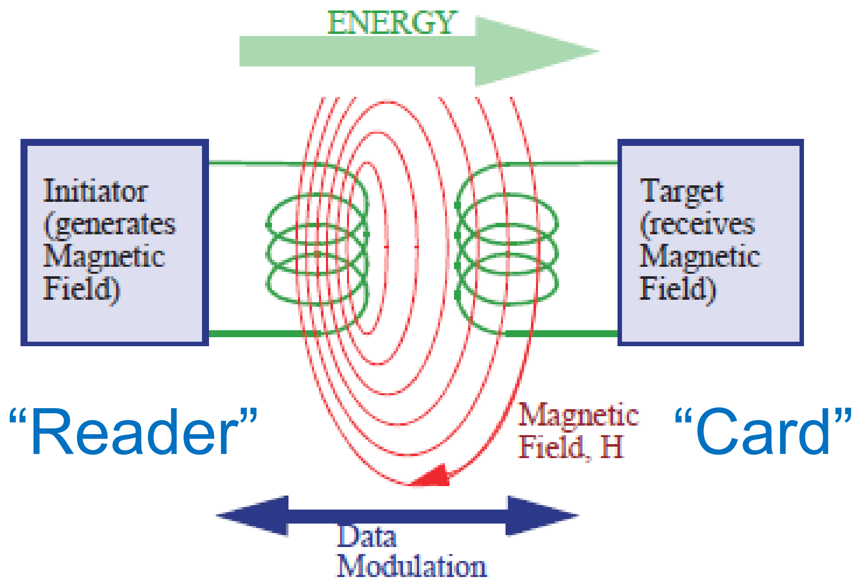
What is NFC?

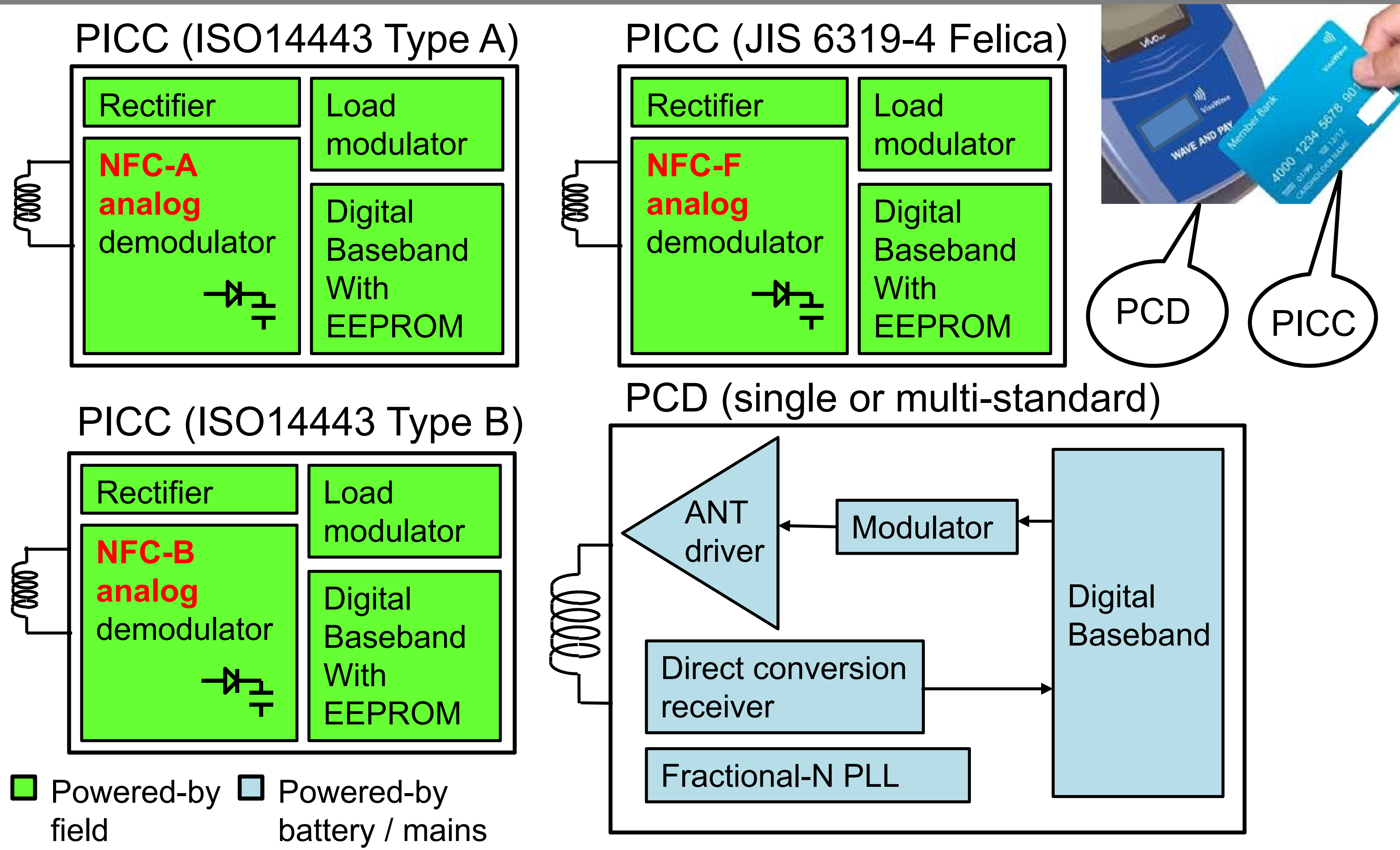
- Near Field Communication
- Short-range, standards-based wireless connectivity technology that enables exchange of data between devices
- Operates in a frequency range centered on 13.56MHz
- Uses magnetic field induction to enable short-range communication (<10cm)
- Use Cases
  - Mobile payment
  - Data Transfer
  - Bluetooth pairing
  - *many others*

What is NFC?



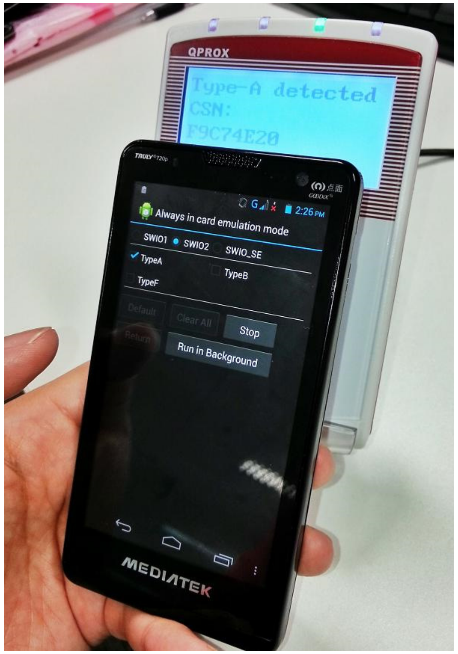
- Reader → Card
  - Energy source for card
  - Data transfer through ASK modulation
- Card → Reader
  - Response through load modulation

Prior NFC days – PCD & PICC



NFC TRX Requirements

- Supports NFC-A/B/F standards in PCD & PICC modes
- Supports variable data transmission rates from 106kbps to 424kbps (NFC Forum) or 848kbps (ISO14443)
- 3 modes of operation
  - Reader/Writer (PCD)
  - Card Emulation (PICC)
  - Peer-to-peer (P2P)
- 2 communication modes
  - Active-passive (conventional)
  - Active-active
- Joint Detection during PICC mode (NFC-A/B/F)
- Supports powered-by-the-field (optional)



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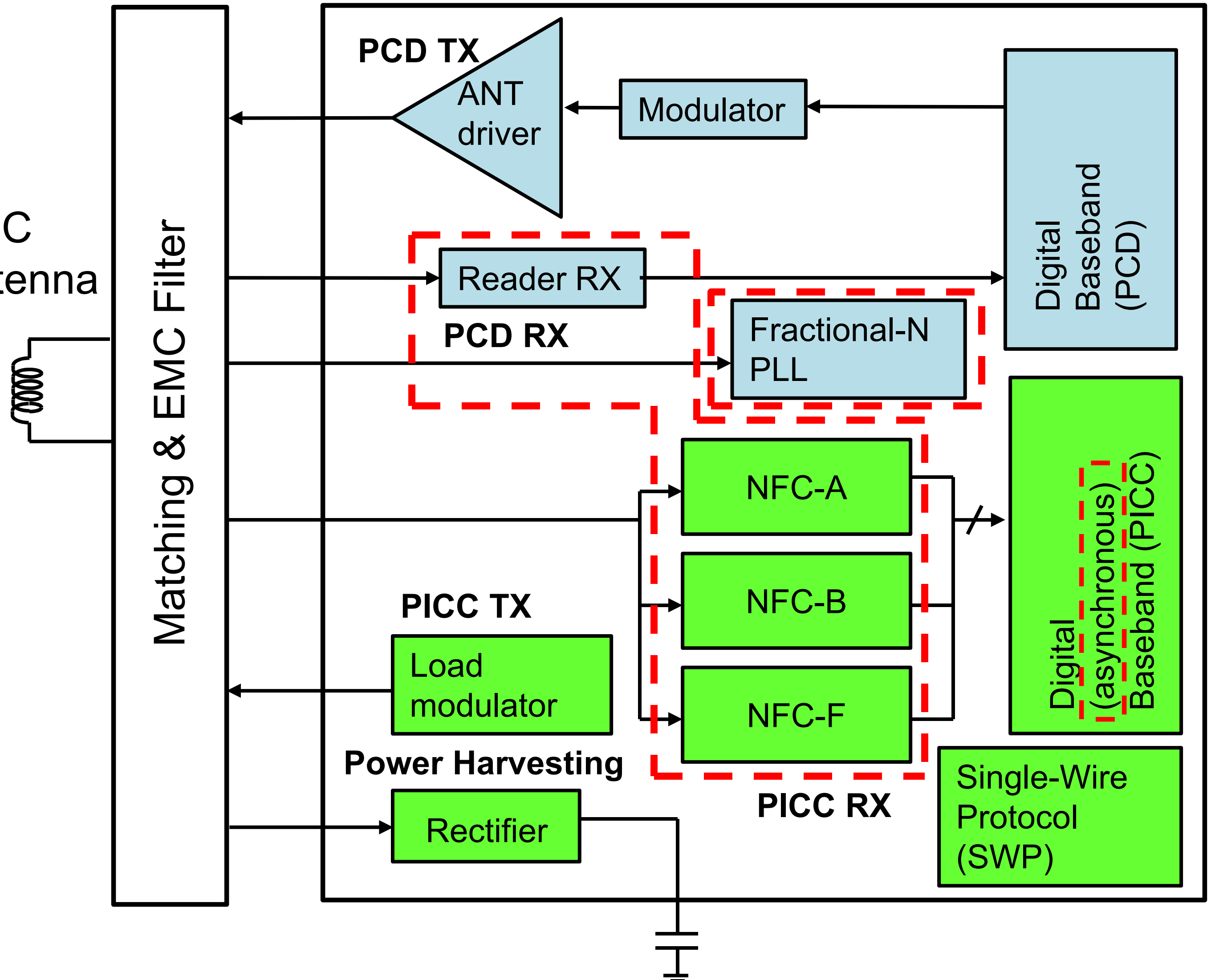
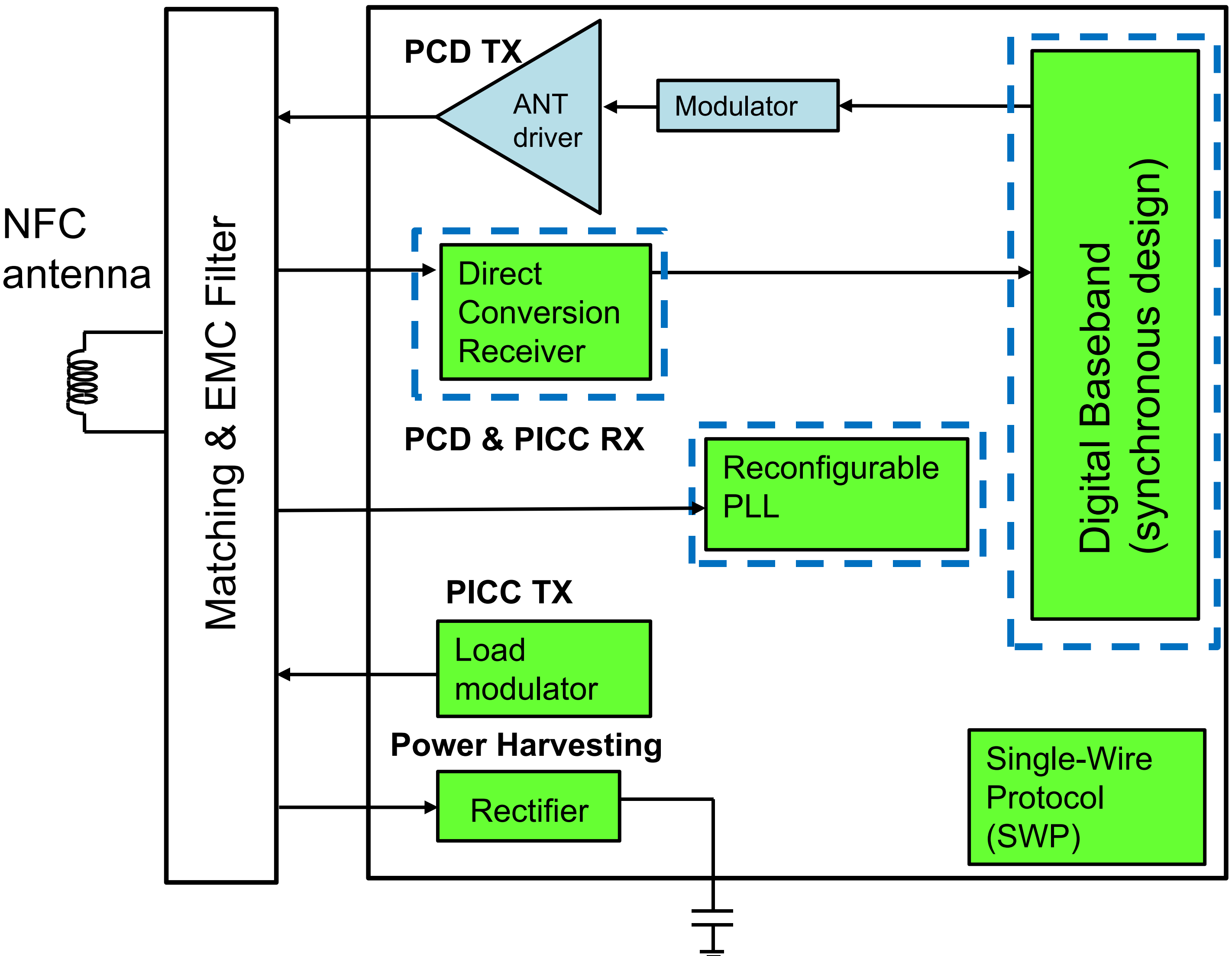
NFC - Conventional Front-End



Merging of PCD & PICC functions with various modes into a single LARGE chip

- Powered-by battery (PCD function)
- Powered-by field capability is preferred (PICC function)

NFC – This Work



- Single-chip with usage of single RX
- Reconfigurable PLL for all modes & standards
- Continuous clock to RX & digital BB

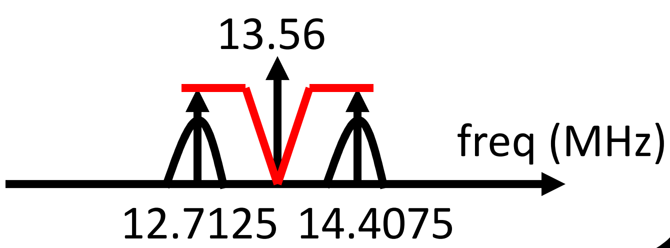
Powered-by battery (PCD function)

Powered-by field option is supported

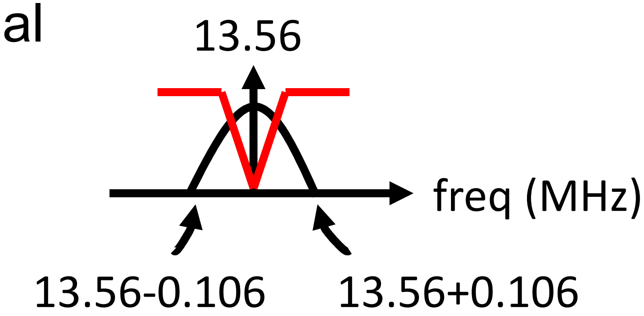
Challenges (Single RX)

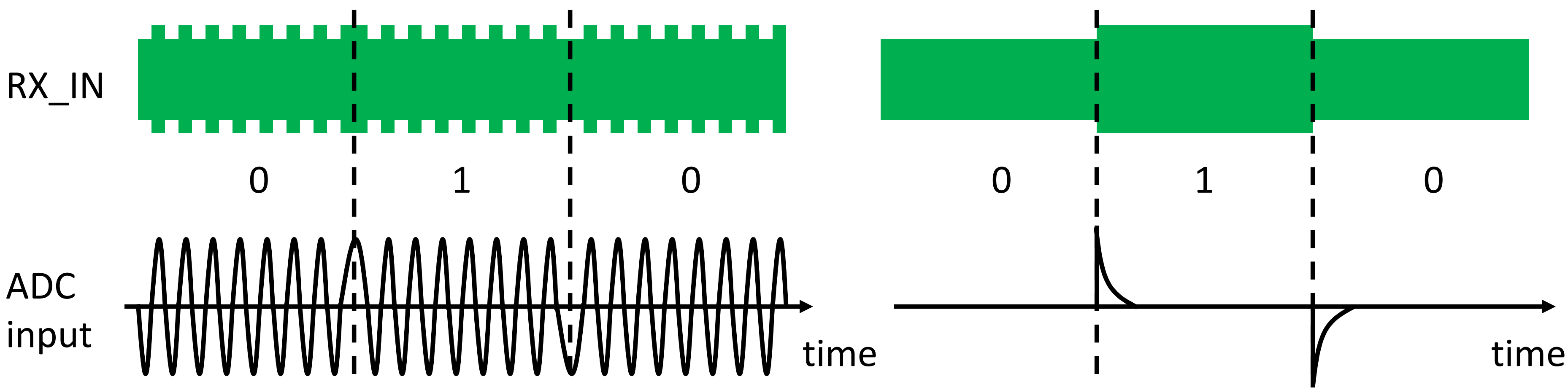
- Impact of HPF on signal reception

PCD receiving NFC-B LM signal (OK)



PICC receiving NFC-B 10% ASK signal



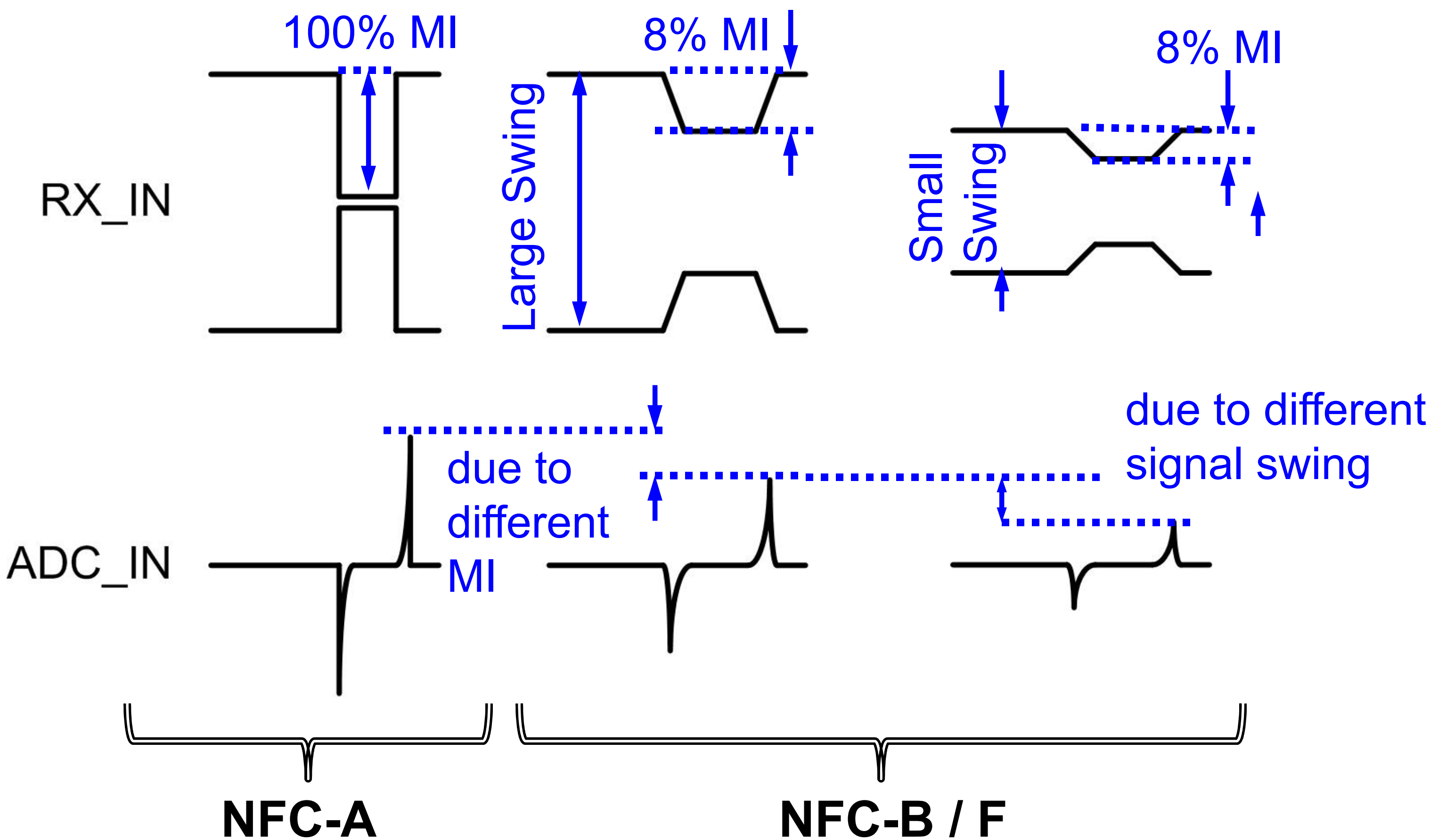


Automatic Gain Control (AGC) based on signals levels at sub-carrier

AGC is not possible. Need to use a fixed RX gain

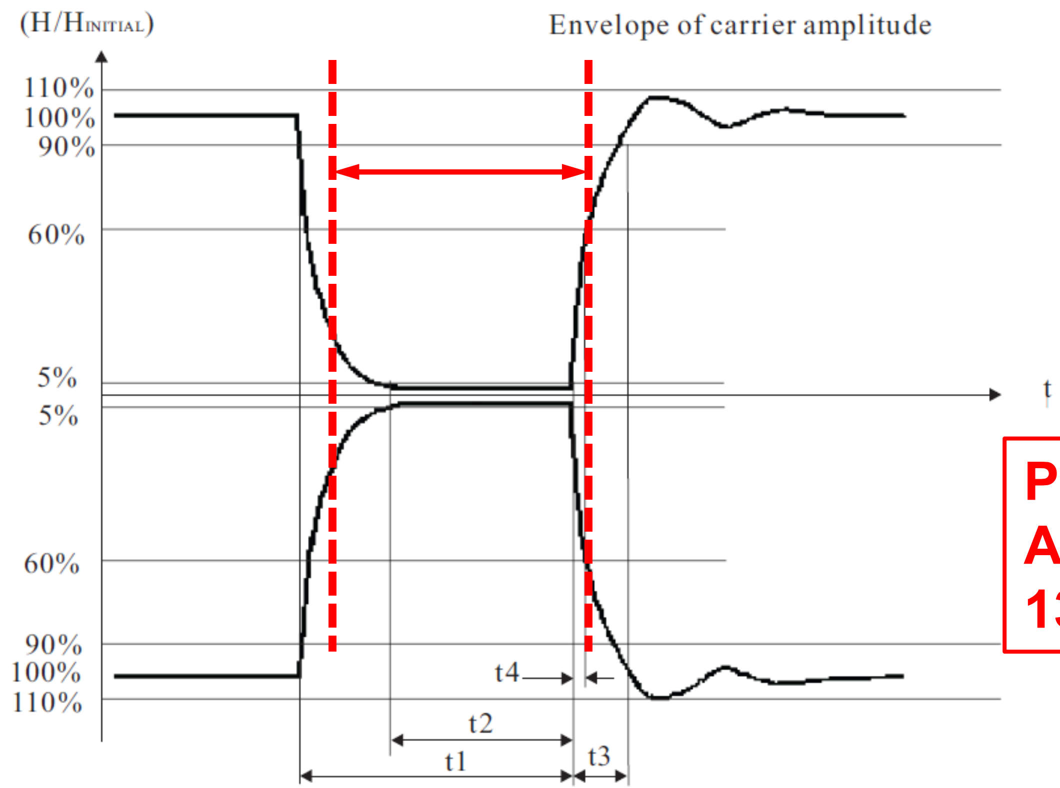
Challenges (Single RX)

- Impact of different standards and signal swing on PICC signal reception



Challenges (Synchronous BB)

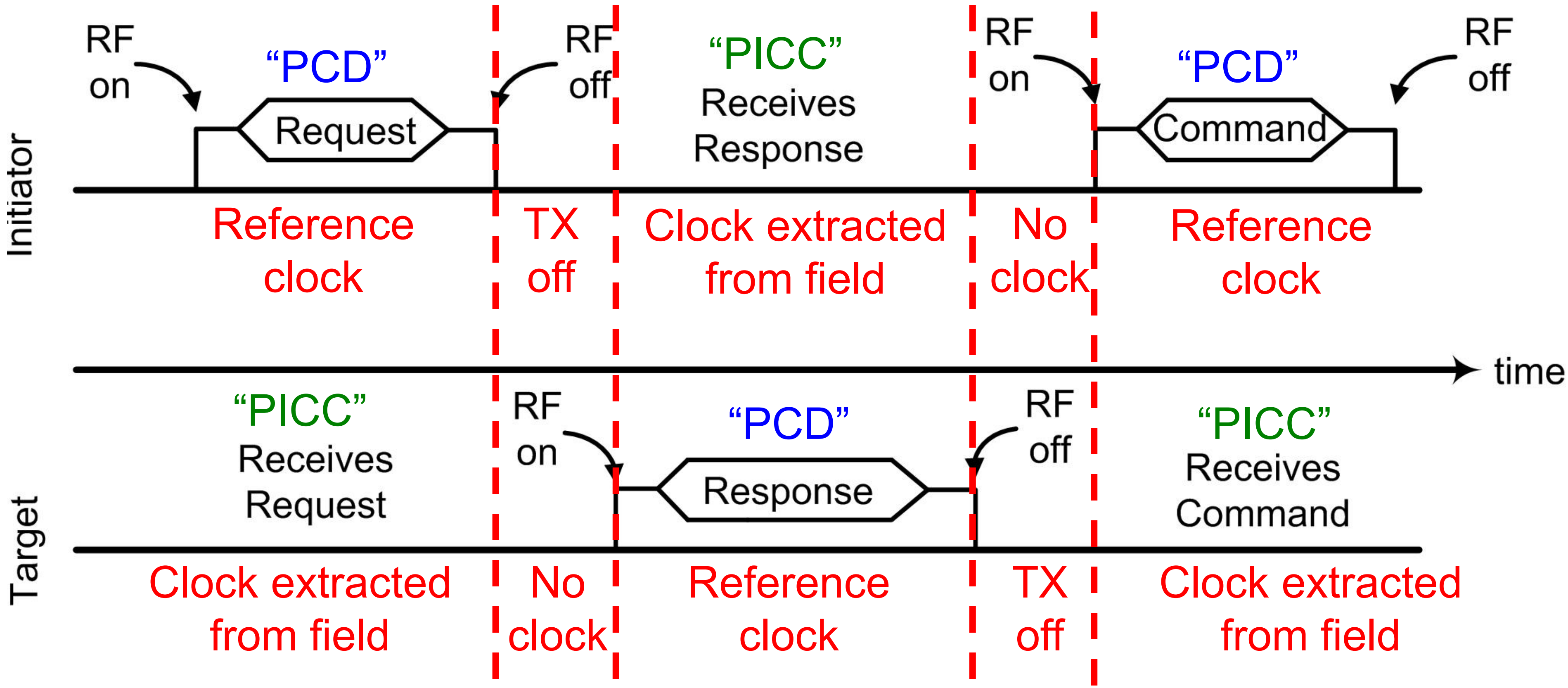
- Absence of carrier during 106kbps NFC-A pause period
  - No continuous clock for DBB
  - No LO signal for direct conversion receiver & ADC



Pause period = Absence of 13.56MHz carrier

Challenges (Multi-mode PLL)

- Different PLL modes required during different phases of P2P active communications



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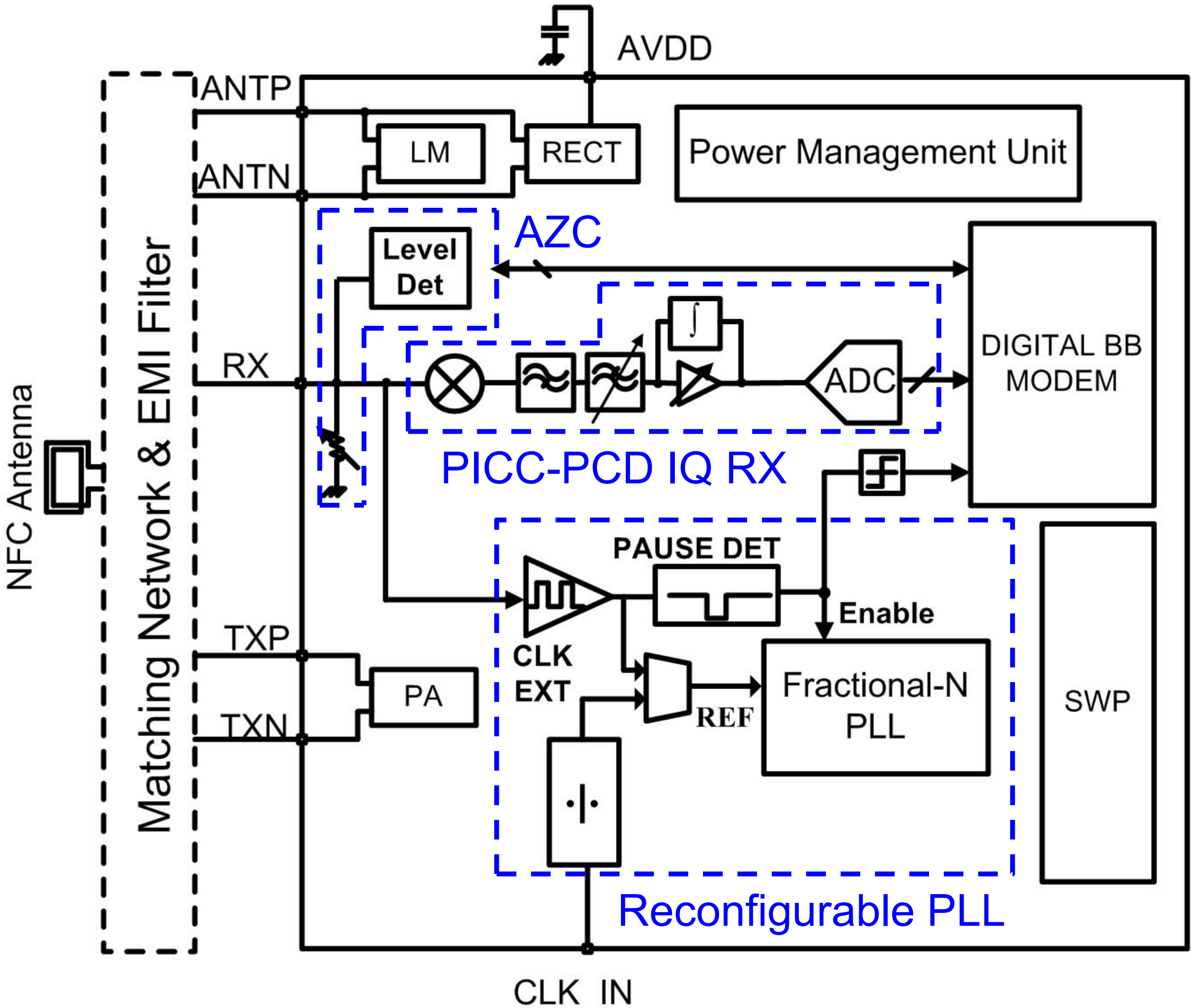
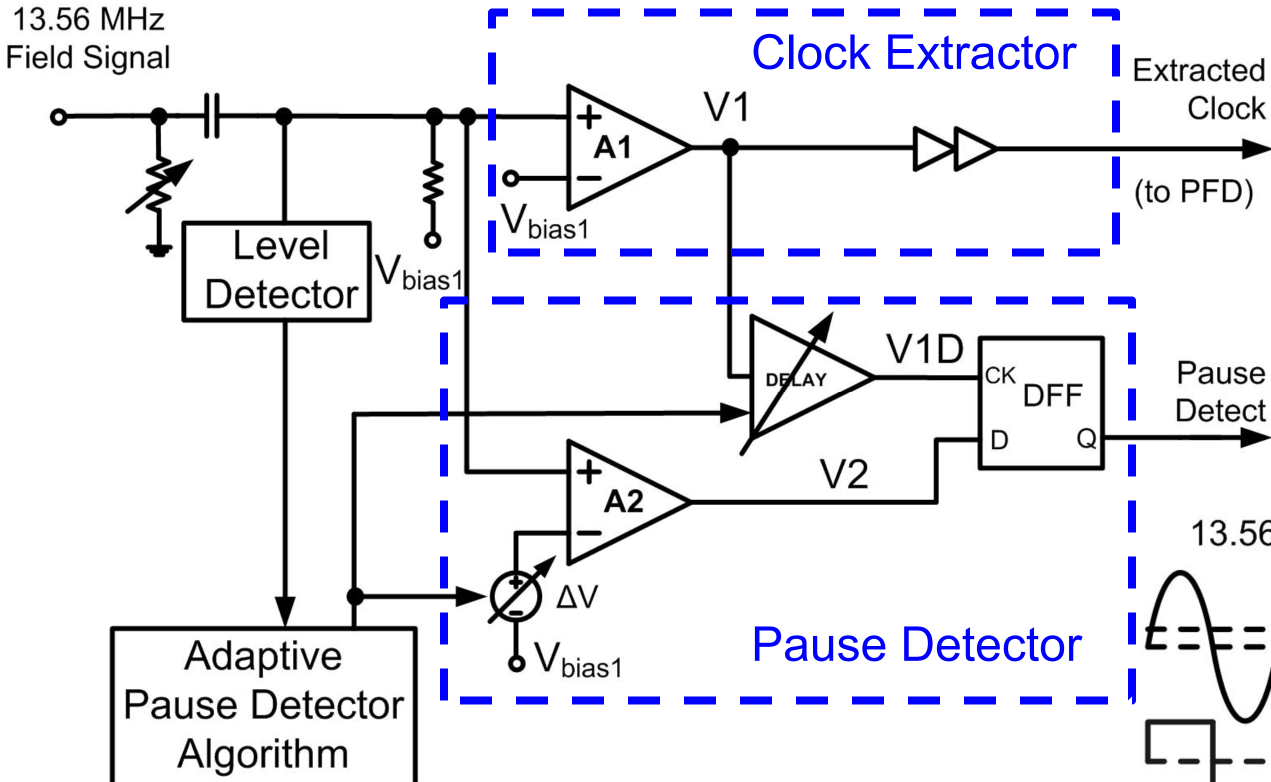
Proposed Solution

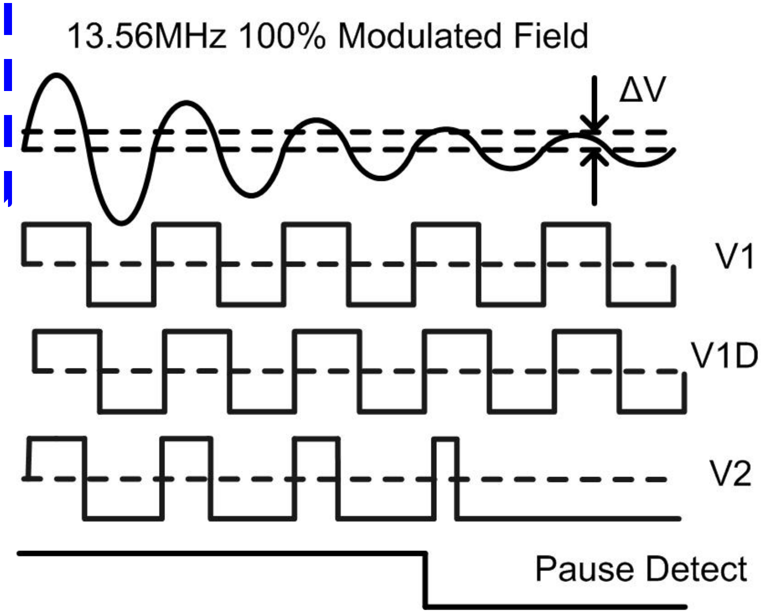


- Single RX for all modes
- Automatic input impedance control (AZC)
- Clock extractor & Pause detector as building block of clock recovery & NFC-A demodulator
- Reconfigurable PLL provides continuous clock for all modes

Clock Extractor & Pause Detector

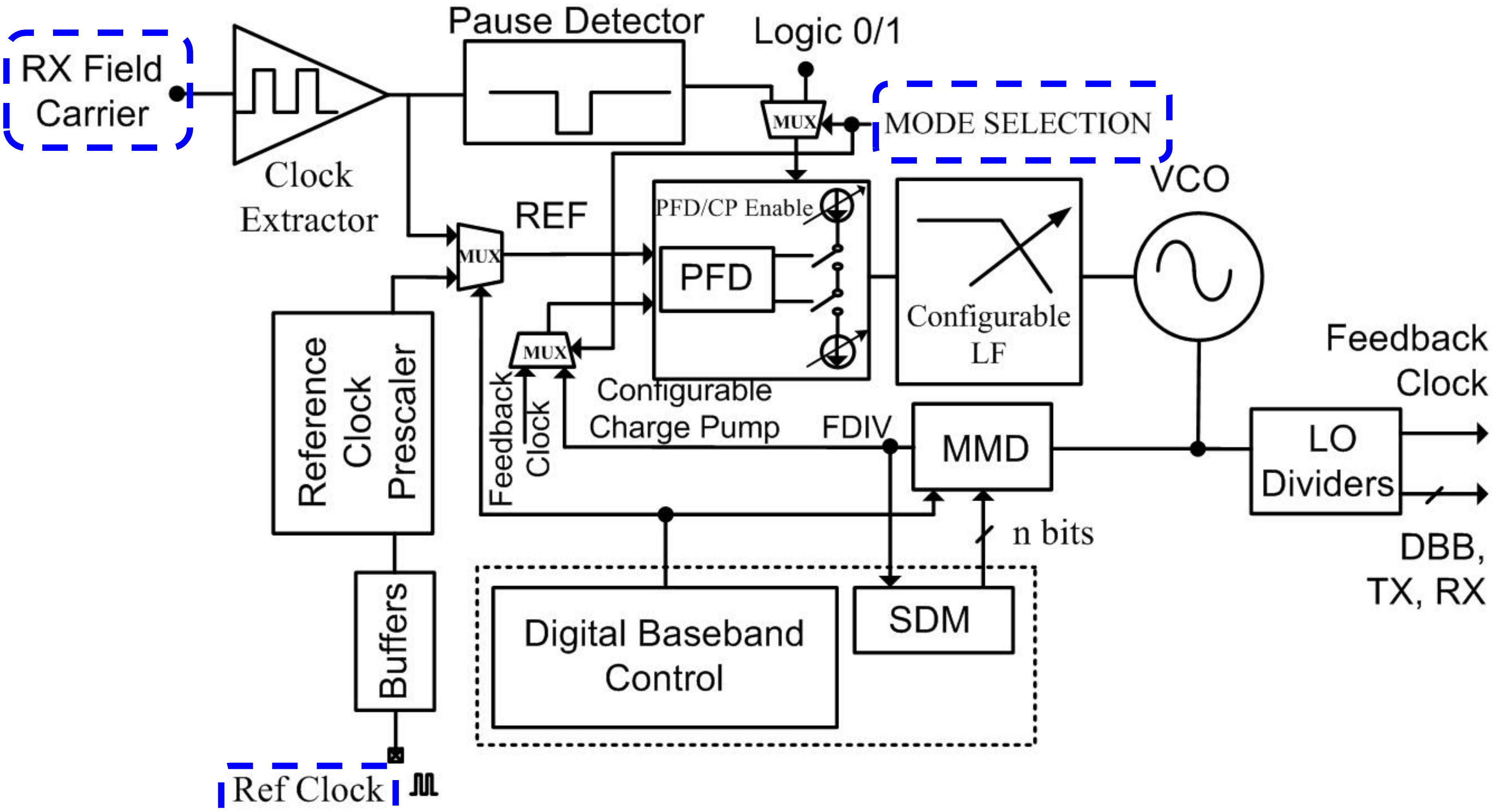


- Clock extractor amplifies the clock from incoming field and send to PFD and Pause Detector

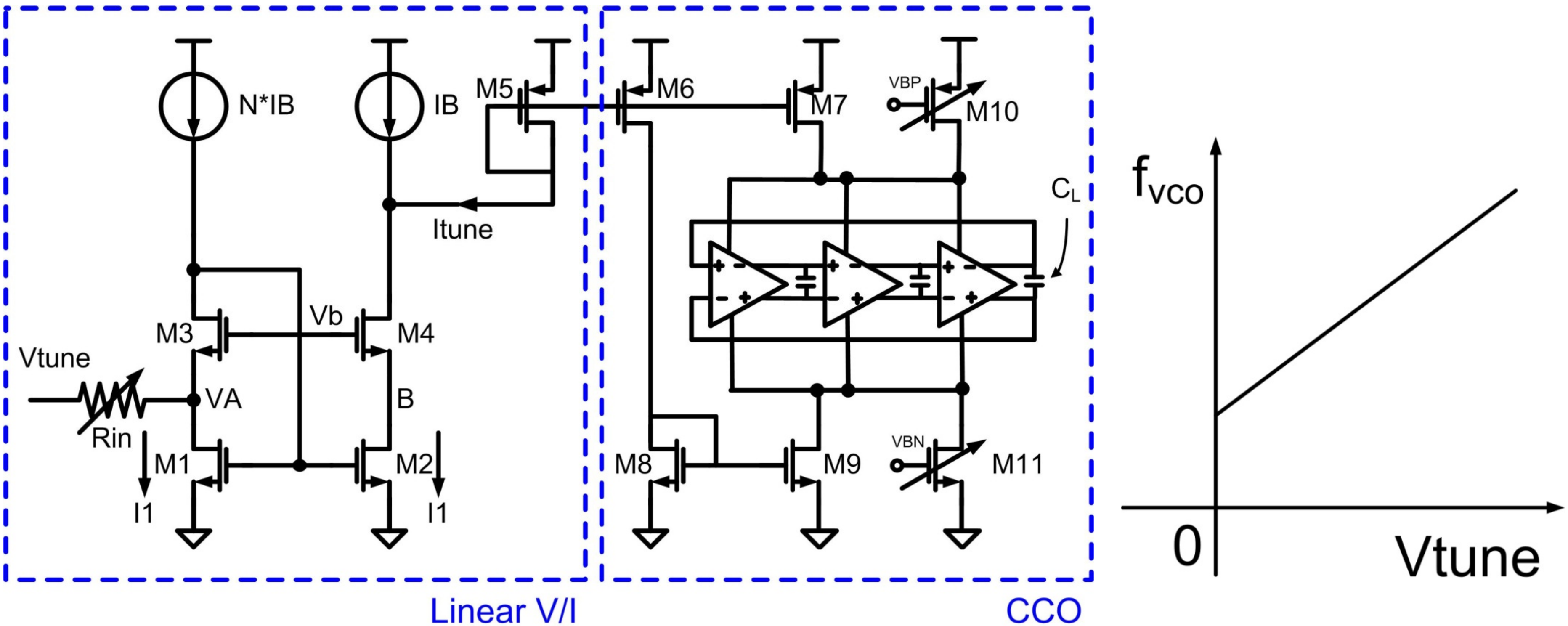


- Pause detector module to overcome the challenge of pause period during NFC-A
- Pause detector output also readily serves as demodulated output for NFC-A standard!

Reconfigurable PLL Architecture



Ring VCO with V-to-I tuning circuit

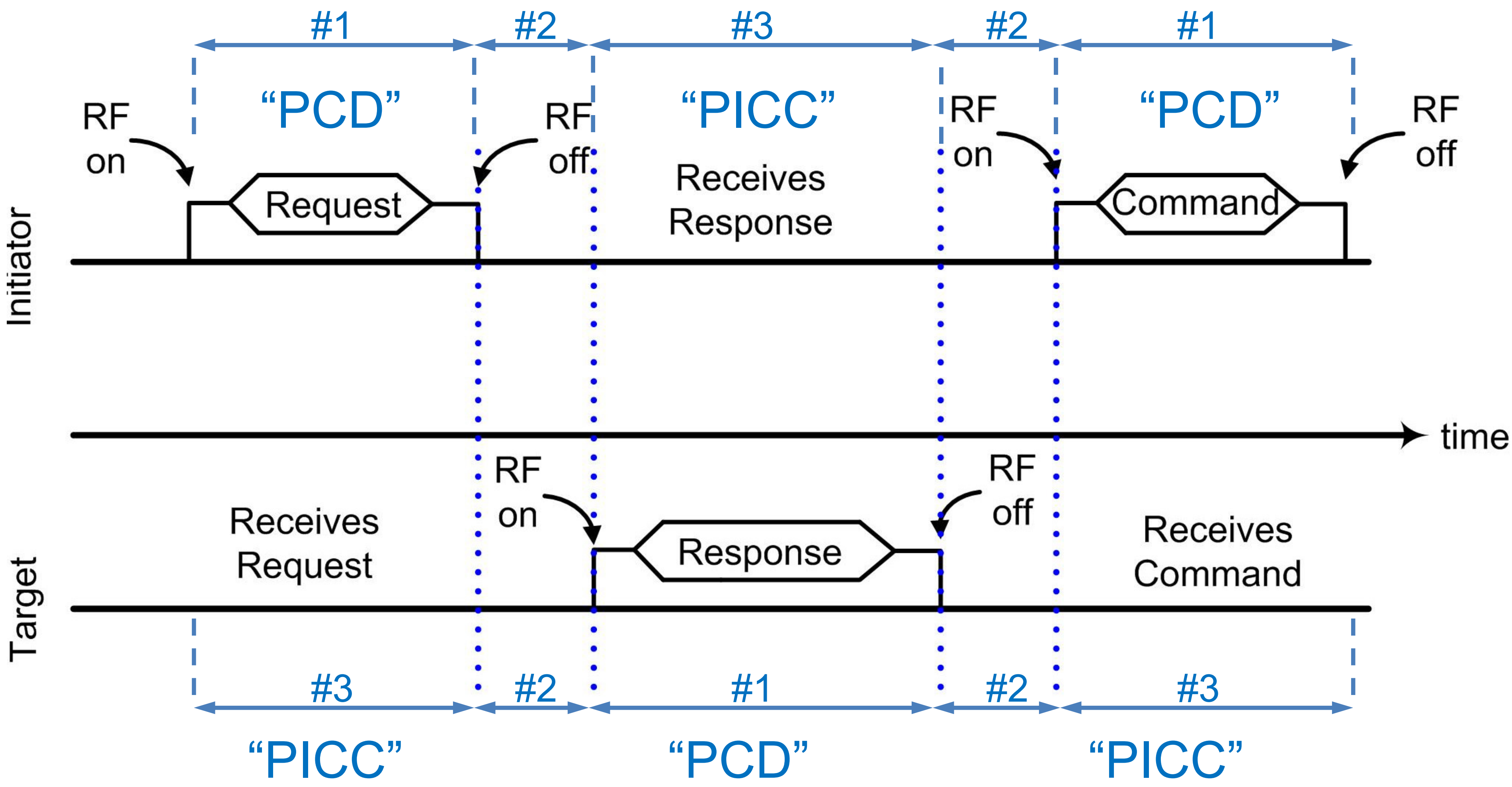


- Linear V-to-I stage, followed by current controlled oscillator

$$f_{VCO} = \frac{Vtune}{3C_L(VDD - VSS)Rin} + \frac{(N-1)IB \times Rin - VA}{3C_L(VDD - VSS)Rin}$$

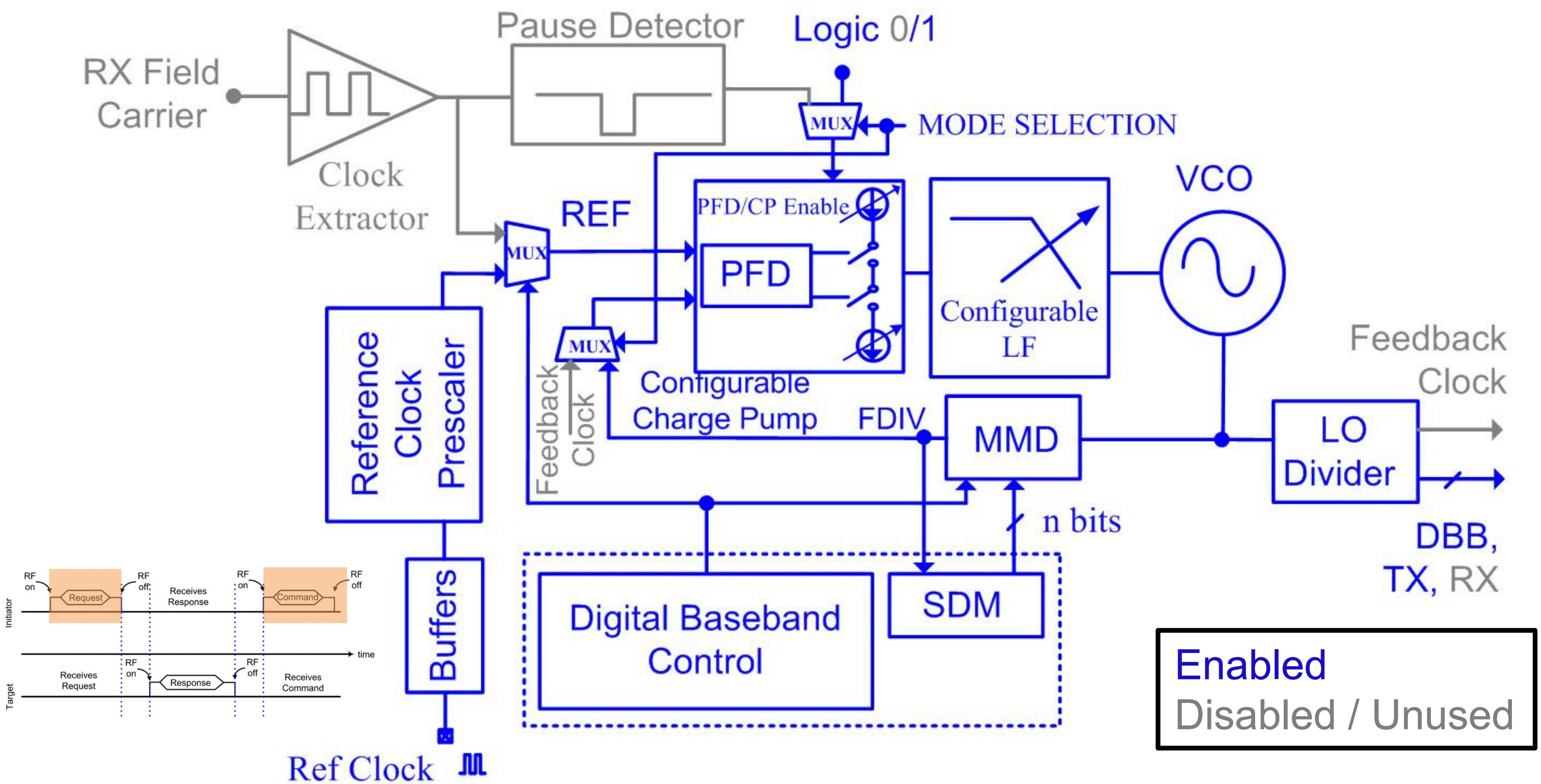
- LO PN @ 848kHz < -124dBc/Hz

Peer-to-peer (active) mode



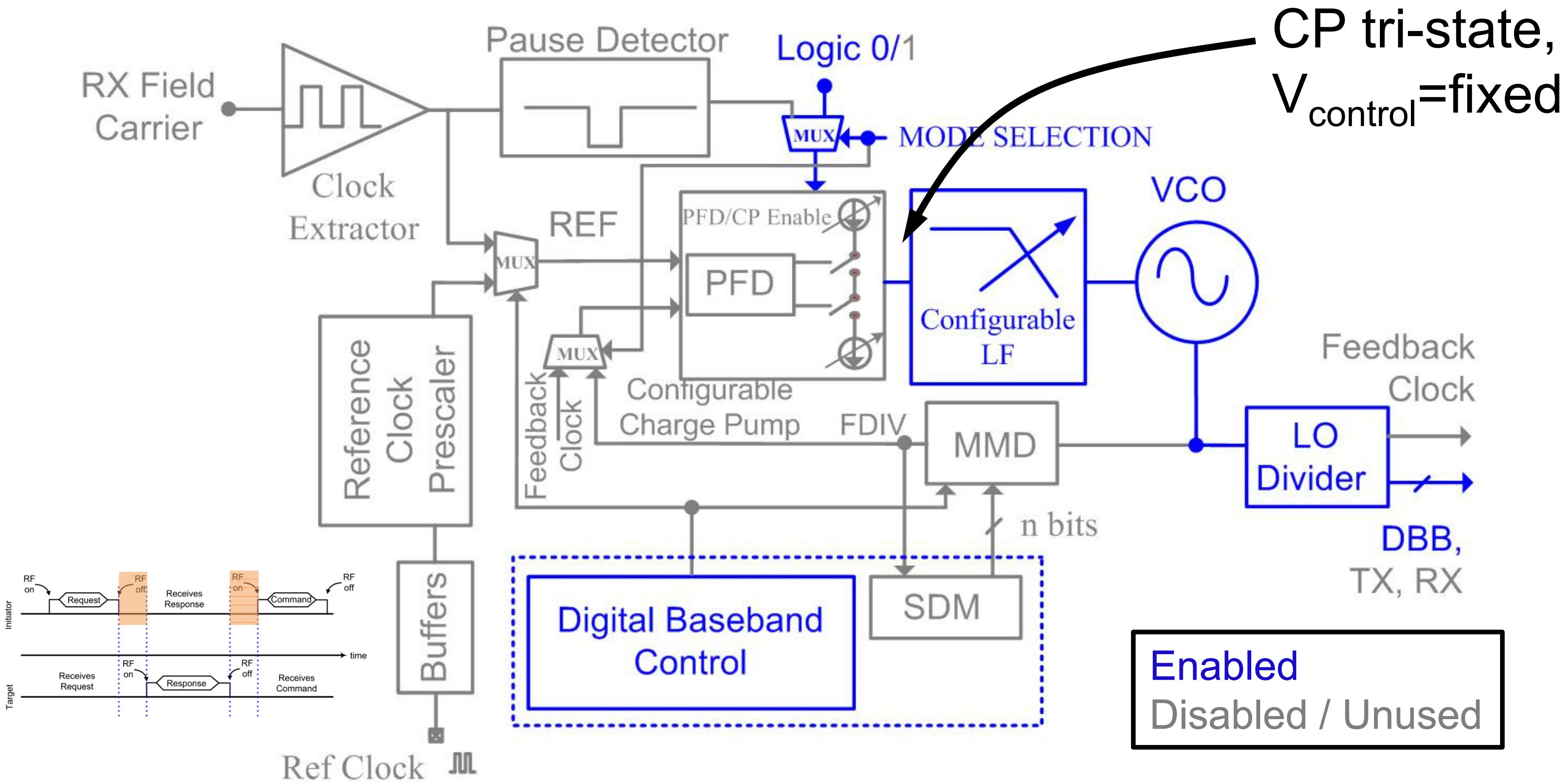
- Agile PLL reconfigured to meet requirements during different phases

Initiator sending commands (#1)



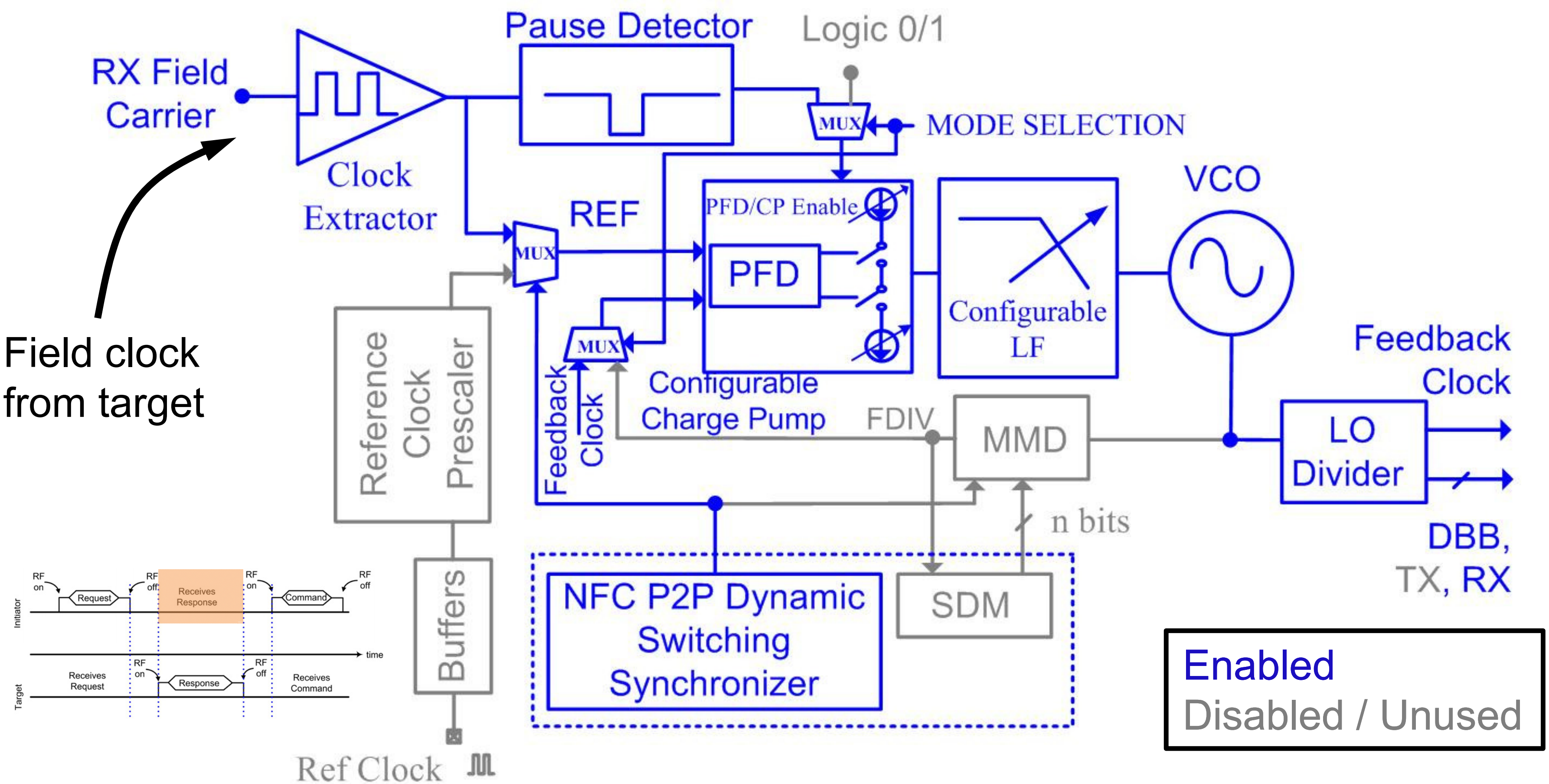
- PLL configured in fractional-N mode for TX data transmission (closed-loop)
- Clock extractor and Pause Detector are disabled

Initiator during field absence (#2)



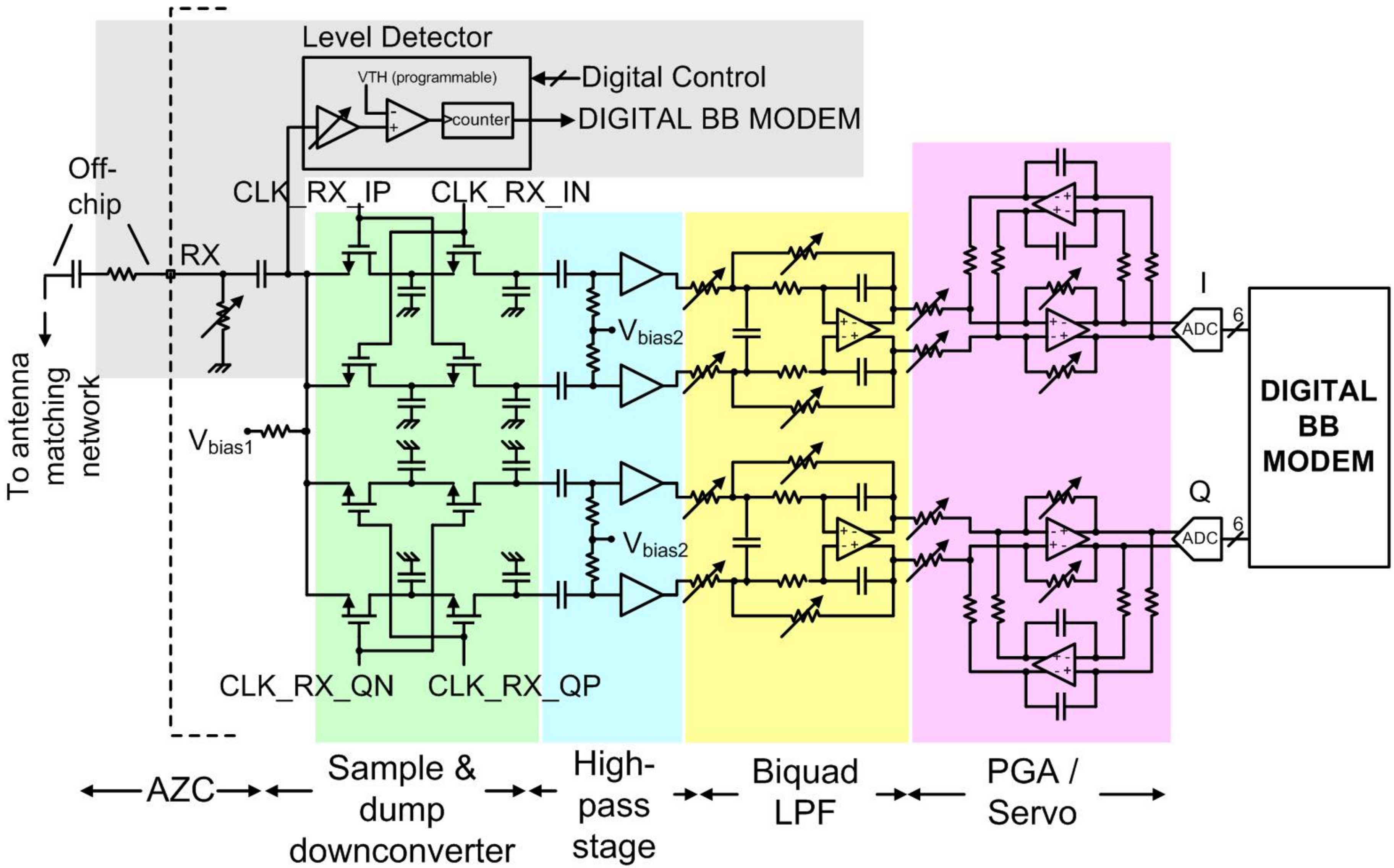
- Charge pump tri-state, VCO held at Vtune voltage (PLL open-loop)
- VCO maintains oscillating voltage at 162.72MHz

Initiator receiving commands (#3)

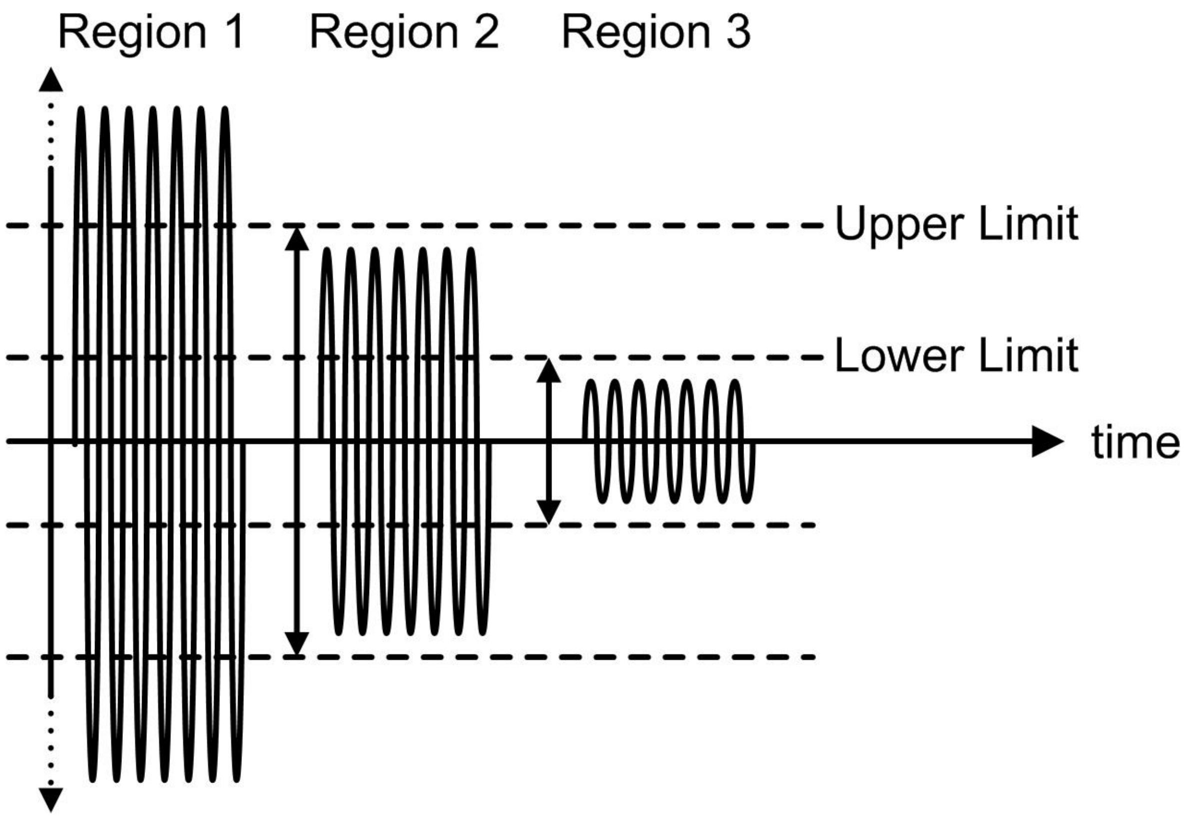


- Clock extractor and Pause Detector are enabled
- Synthesizer configured as int-N PLL with 13.56MHz field clock (from extractor) as the reference clock (closed-loop)

RX Architecture

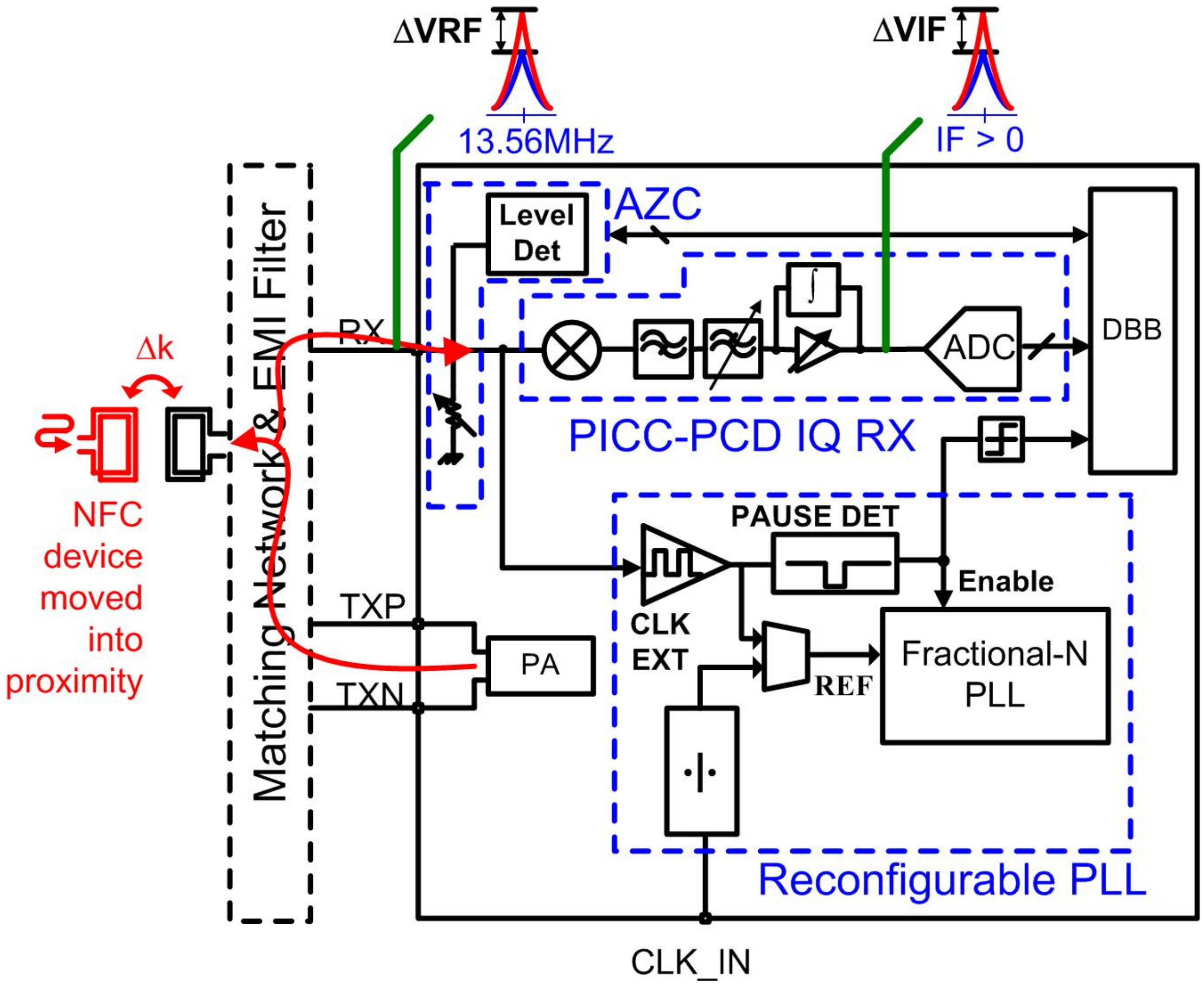


AZC



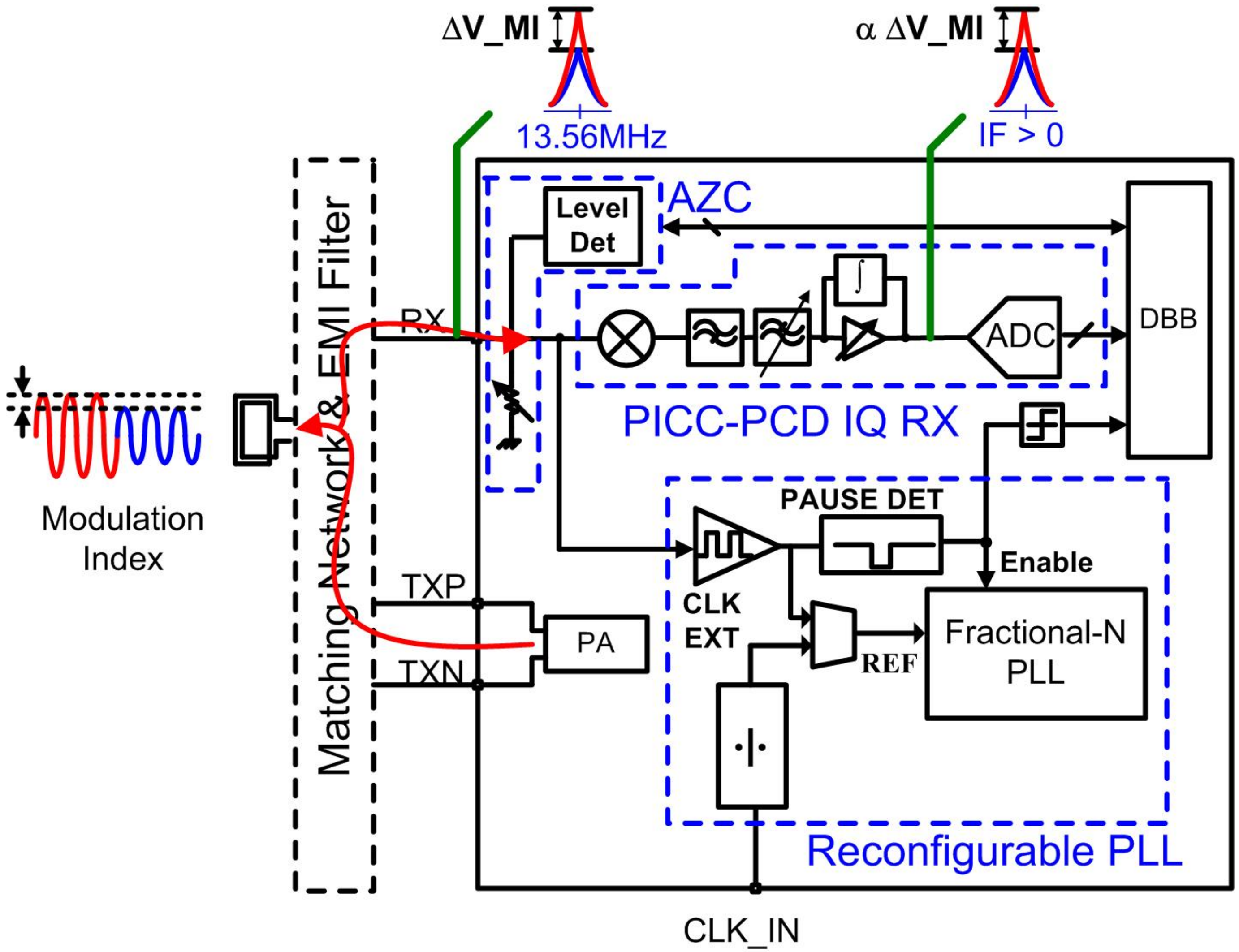
- Automatic (input) impedance control
- Used in PICC mode during initial field
- Obtains signal level from Level Detector
- Increases attenuation to achieve desired input swing range

Reader Low Power Polling



- Turns on TX for a very short duration (sub ms)
- Loop-back TX-to-RX scheme
- Re-configurable PLL brings RX to a **low-IF architecture**
- Digital BB decode the change in amplitude level.
- Wakes up reader to a full-power polling mode.

TX Modulation Index Calibration



- Applies to TX Poller for NFC-B and F
- Same loop-back TX-to-RX scheme
- Re-configurable PLL brings RX to a **low-IF architecture**
- TX level adjusted to meet desired modulation index

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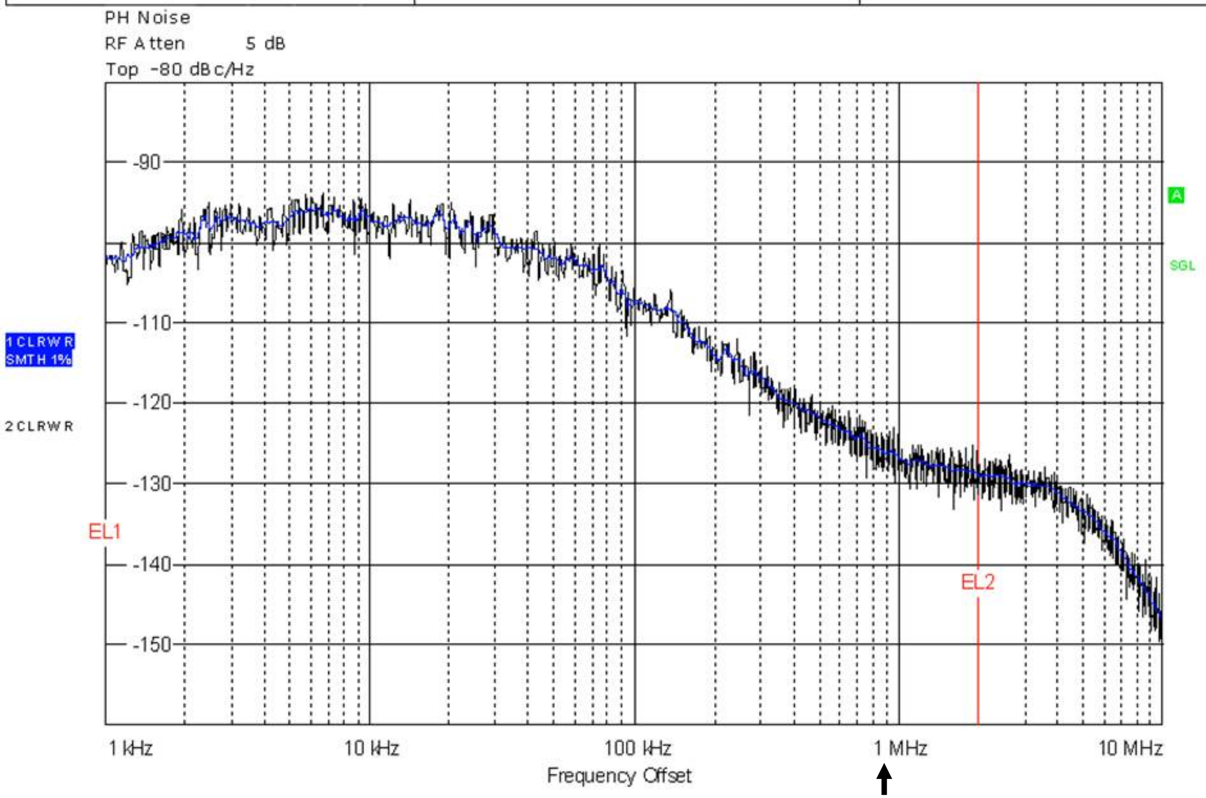
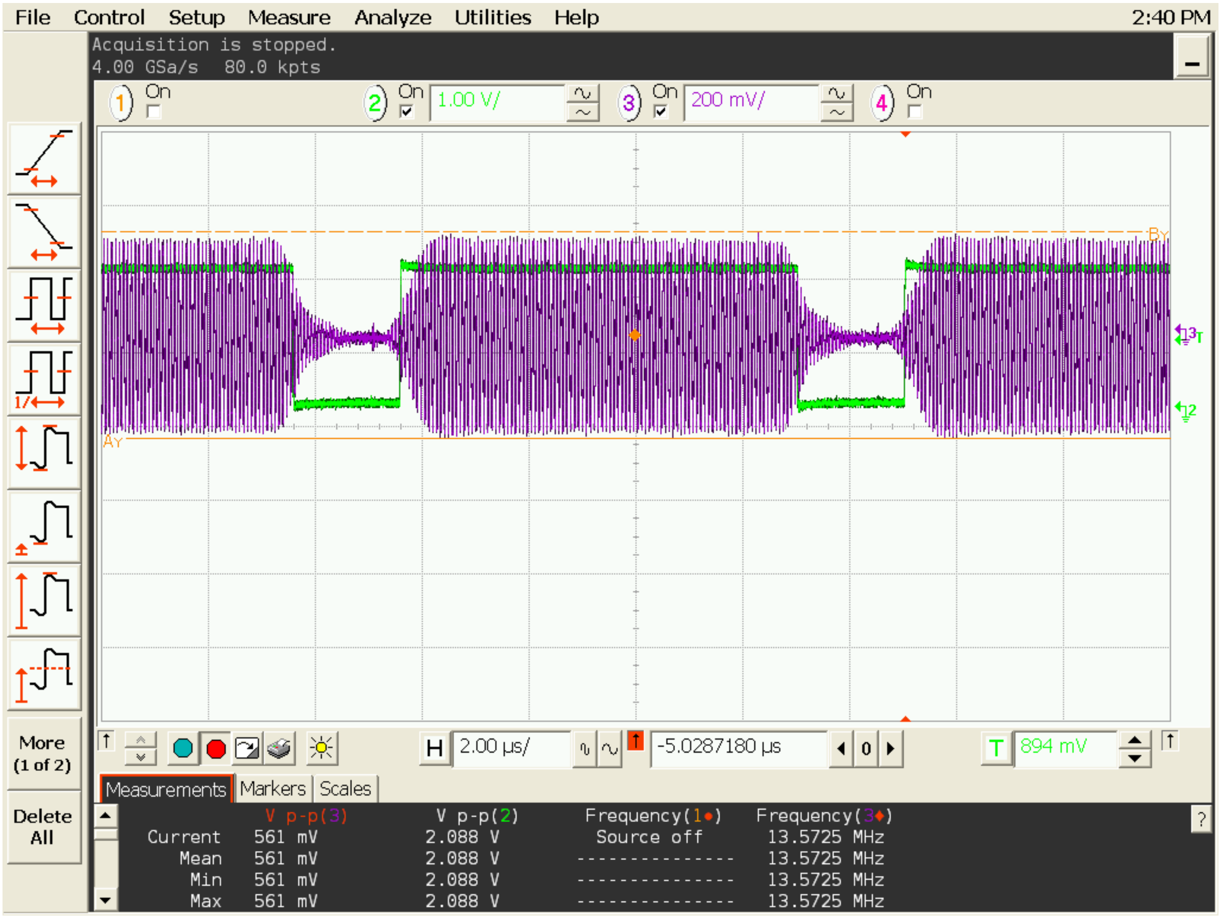
Ring Osc Phase-Noise

PHASE NOISE					
Settings		Residual Noise		Spot Noise [T1]	
Signal Freq:	13.559999 MHz	Evaluation from 1 kHz to 2 MHz		1 kHz	-101.61 dBc/Hz
Signal Level:	3.24 dBm	Residual PM	0.266 °	10 kHz	-97.24 dBc/Hz
Signal Freq Δ:	0.45 Hz	Residual FM	1.047 kHz	848 kHz	-125.64 dBc/Hz
Signal Level Δ:	-0.35 dBm	RMS Jitter	54.4999 ps	1 MHz	-126.75 dBc/Hz



- LO PN @ 848kHz = -125dBc/Hz during PCD mode

Pause Detector



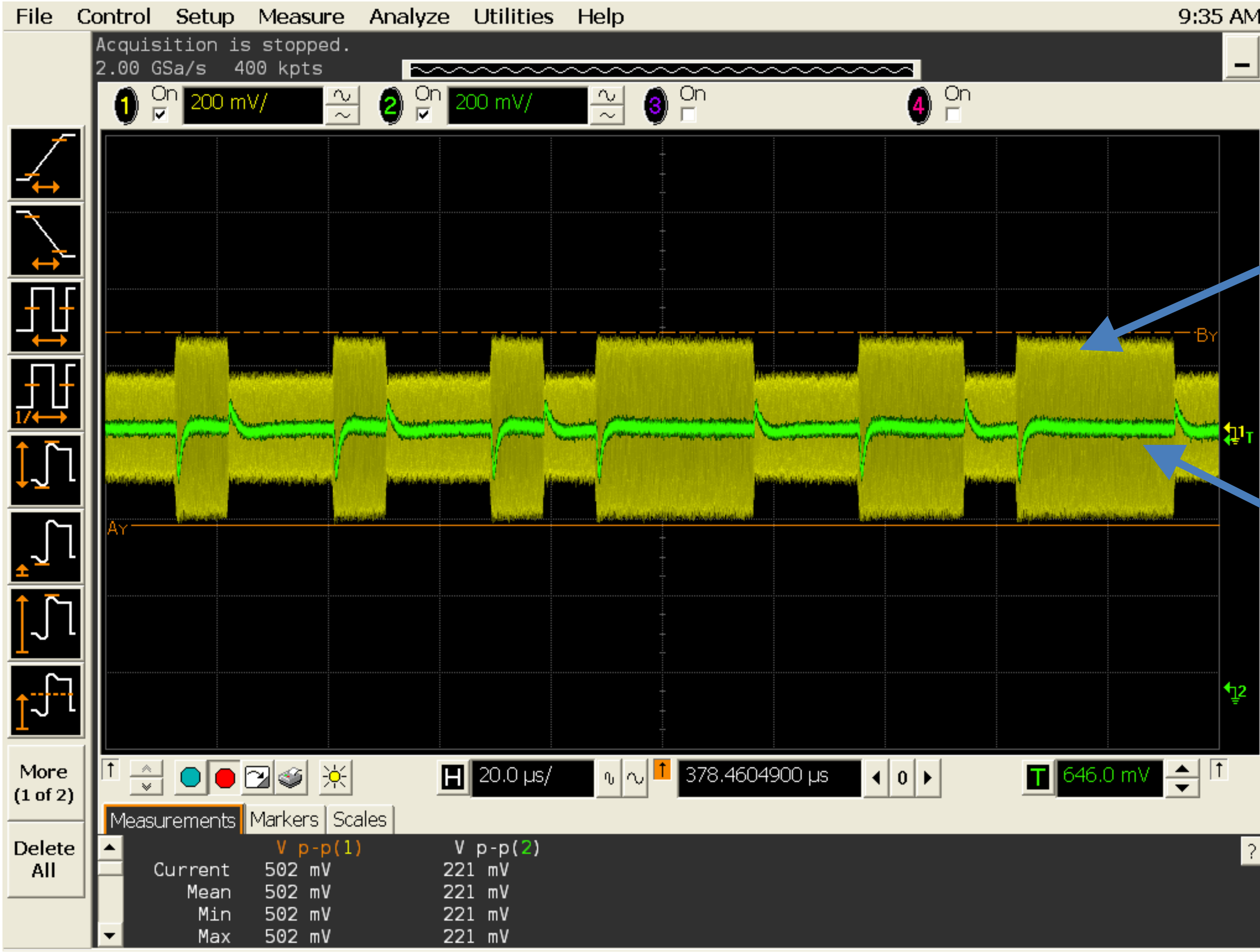
Legend :

Waveform at Receiver input

Pause detector output

- PICC receiving NFC-A signals from reader with 100% modulation index
- Pause detector correctly demodulates data from reader

Received signals from PICC



Waveform at Receiver input

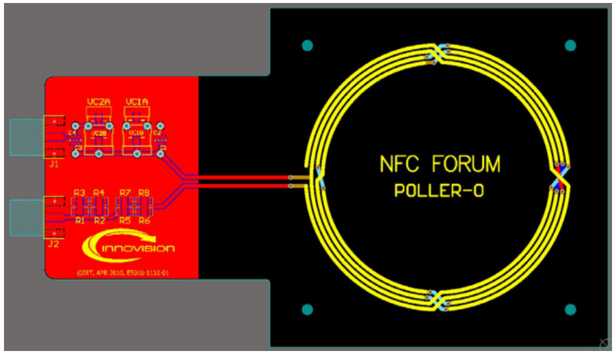
Waveform at PGA output (before ADC)

- PICC mode receiving NFC-B signals (106kbps, 10% modulation index)
- Transitions captured as peaks (rising) & dips (falling) of data waveforms

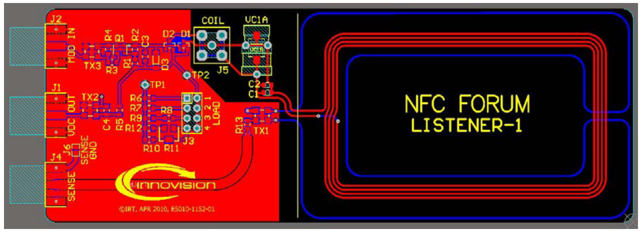
NFC Forum Test

Mode	NFC-x	Reference Device	Distance (cm)
PCD	A	Listener-1 with 820Ω load	5.0
	B		10.3
	F 212 & 424kbps		7.0
PICC	A & B	Poller-0 calibrated to provide nominal power	6.2
	F 212 & 424kbps		5.5

DUT with 50mm x 46mm antenna



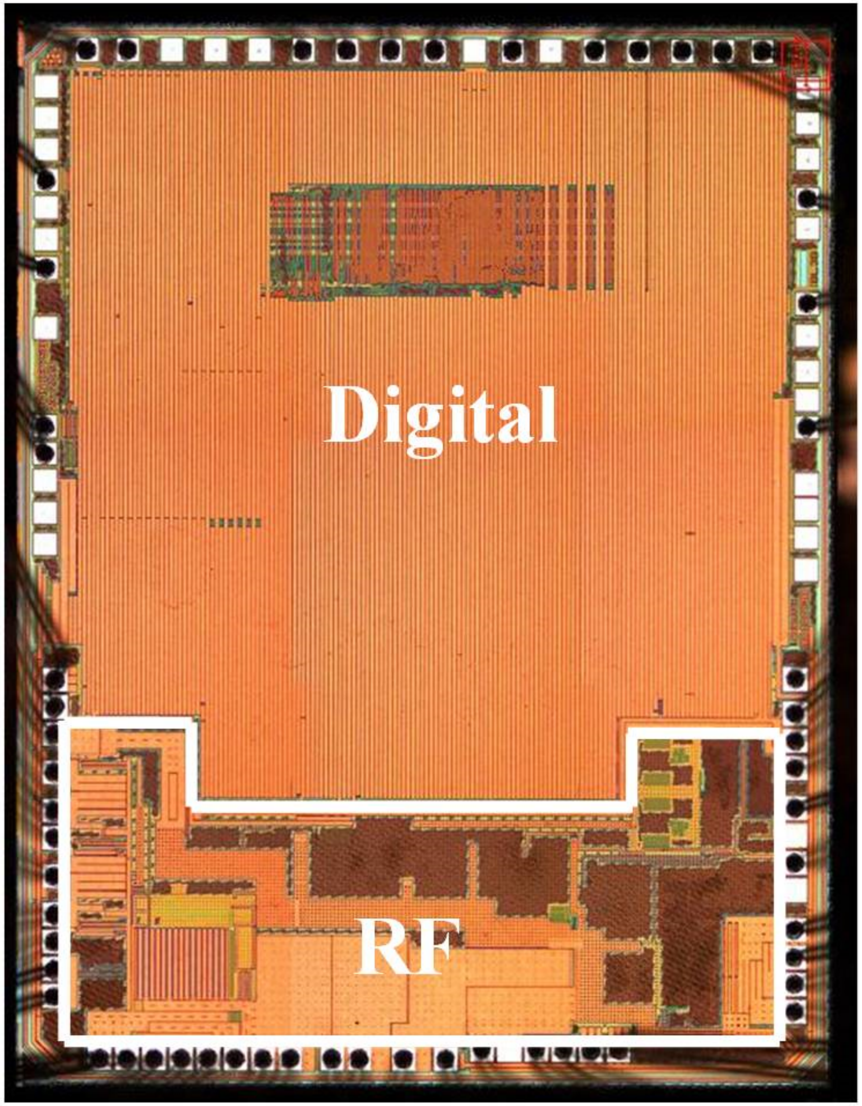
NFC Forum Poller-0



NFC Forum Listener-1

Near Field Communication
CERTIFIED

Die Micrograph



- 0.11μm CMOS
- 32-pin 4mm x 4mm QFN package
- Chip size: 4.7 mm^2
- RF size: 1.1 mm^2
- No on-chip inductors

Comparison with Recent Work

	This Work	ISSCC13 [1]
Technology	110nm CMOS	45nm CMOS
RF + Analog Area	1.1 mm^2	3.4 mm^2
Supported modulation depth range	8%~100%	8%~100%
Supported standards	ISO-14443 ISO-18092 ISO-15693 NFC forum	ISO-14443 ISO-18092 ISO-15693 NFC forum
PLL VCO topology	ring	LC
Reader PA VDD	3.3V	NA
Digital Supply voltage	1.2V	1.0V
Analog Supply voltage	1.8/1.5 V	1.8
PICC mode SoC current	3.5mA	4mA
Max. reader drive current	250mA	200mA
Card detection loop average supply current	70µA	N/A
Communication distance (P2P, PCD & PICC)	≤5cm	N/A
ESD	+/-3kV HBM, +/-300V MM, +/-500V CDM	+/-2kV HBM, +/-500V CDM

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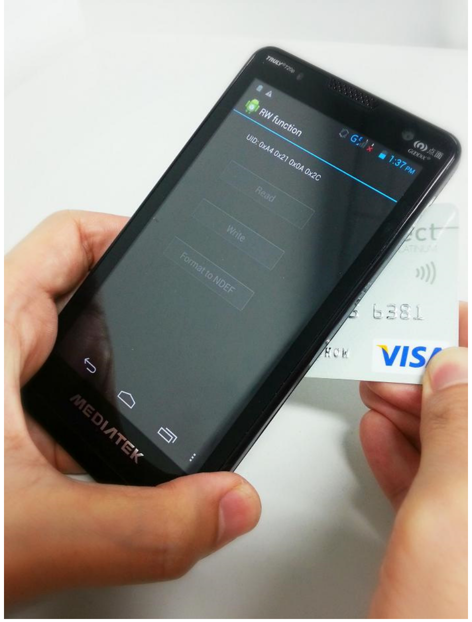
Conclusion

- Single direct conversion RX for PCD and PICC modes
  - Receive load modulated signals (PCD mode), and different ASK signals (PICC mode)
  - Pause detection circuit allows NFC-A (100% ASK) to be demodulated
  - AZC to prevent NFC-B & F signals from saturating ADC
- Reconfigurable PLL
  - Uses ring VCO that meets PN requirements
  - Supports all requirements in triple-modes (PCD, PICC, P2P Initiator & Target) with synchronous DBB implementation
- Modulation Index Calibration and Low Power Polling
  - Utilizes the same hardware (PLL reconfigured, allowing RX in LIF) to allow both NFC supporting schemes to work
- Total TRX+PLL+PMU+SWP area : 1.1mm^2 in 110nm process

Acknowledgement

MediaTek

- Wireless Connectivity & Networking Business Unit
- Communication System Design team
- Manufacturing Department



A 13.3mW 500Mb/s IR-UWB Transceiver with Link-Margin Enhancement Technique for Meter-Range Communications

Shuli Geng, Dang Liu, Yanfeng Li, Huiying Zhuo, Woogeun Rhee, Zhihua Wang

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  - HDR transmission in IR-UWB
  - Enhanced link margin with FH
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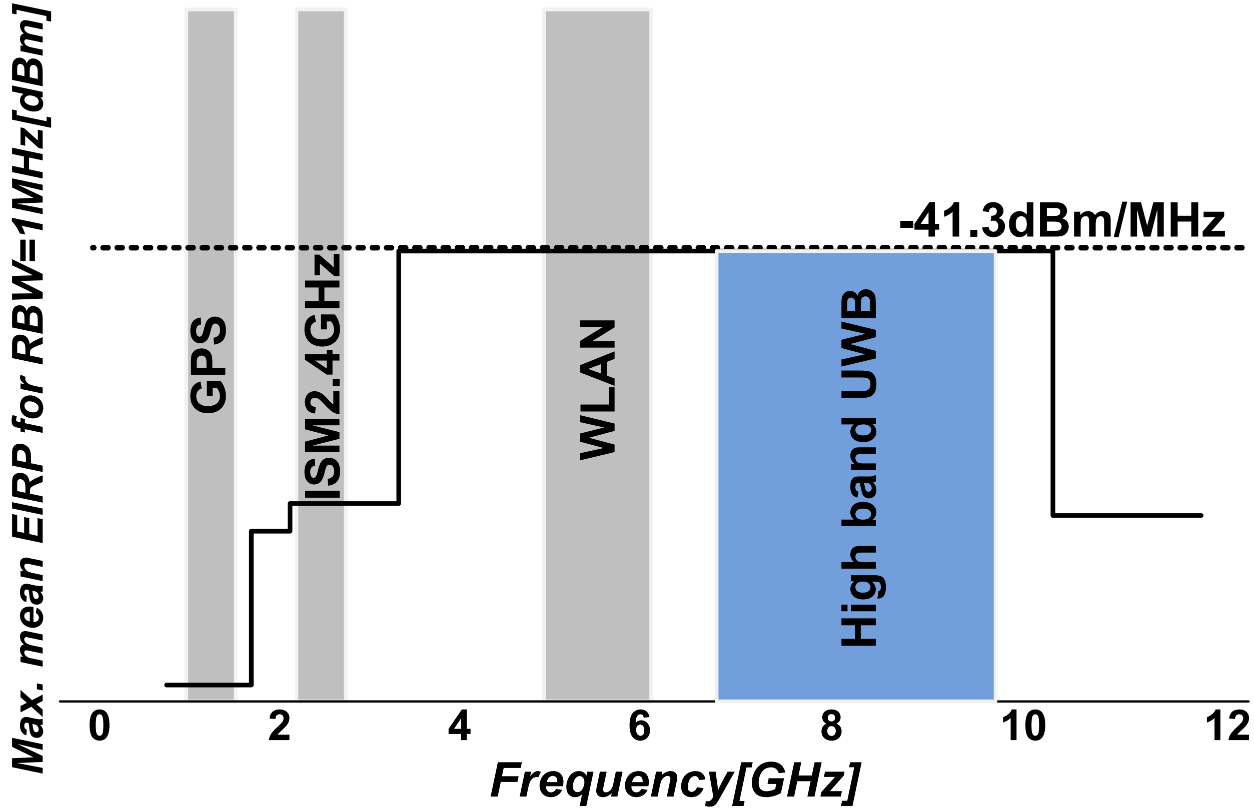
Wireless Operating Room

(UWB Ultrasound System [6])

(source: NDSsi white paper)

- Wireless technology into medical OR
  - Needs stable transmission for 1-5m range.
  - HDR transmission can relax coding complexity.

UWB for Wireless OR



- Seamless transmission with 75nW/MHz power
  - Bluetooth or WiFi for bidirectional backchannel data
- Enables frequency reuse in different ORs.
- Flexible data rate for various imaging

Non-coherent IR-UWB for HDR

IR-UWB

FM-UWB
- ✗ Low data rate
- ✗ No duty cycle
- ✓ Good spectrum
- ✓ Low peak power

Coherent IR-UWB
- ✗ Power hungry LO
- ✗ Synchronization at picosecond
- ✓ Higher sensitivity, support BPSK

Non-coherent IR-UWB
- ✓ No LO, self-mixing
- ✓ Synchronization at symbol-level, at nanosecond
- ✓ Low complexity
- ✗ Low sensitivity, OOK/PPM

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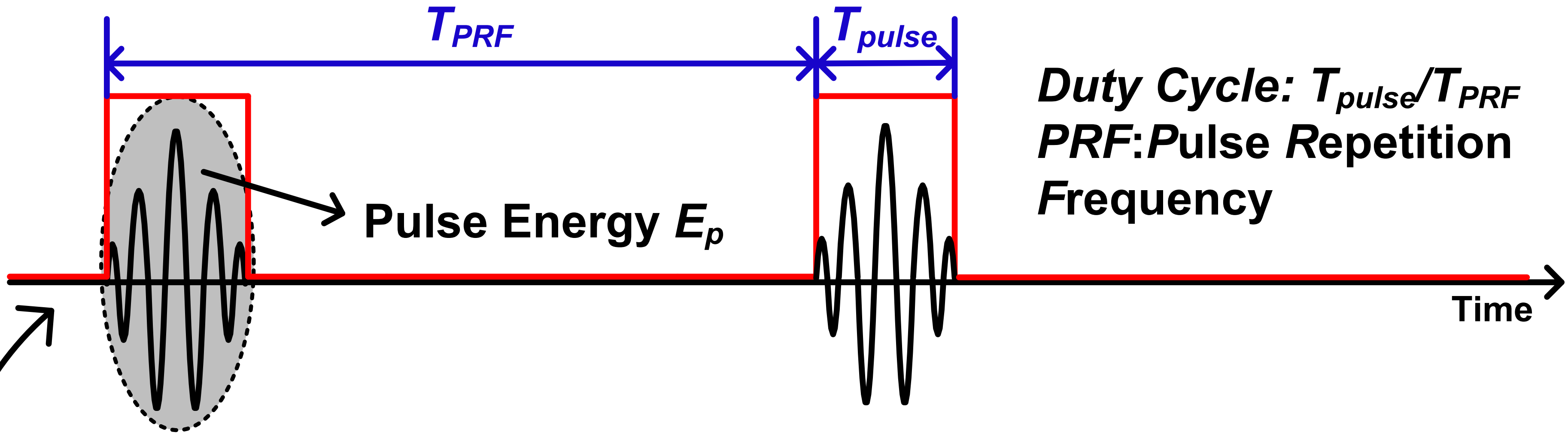
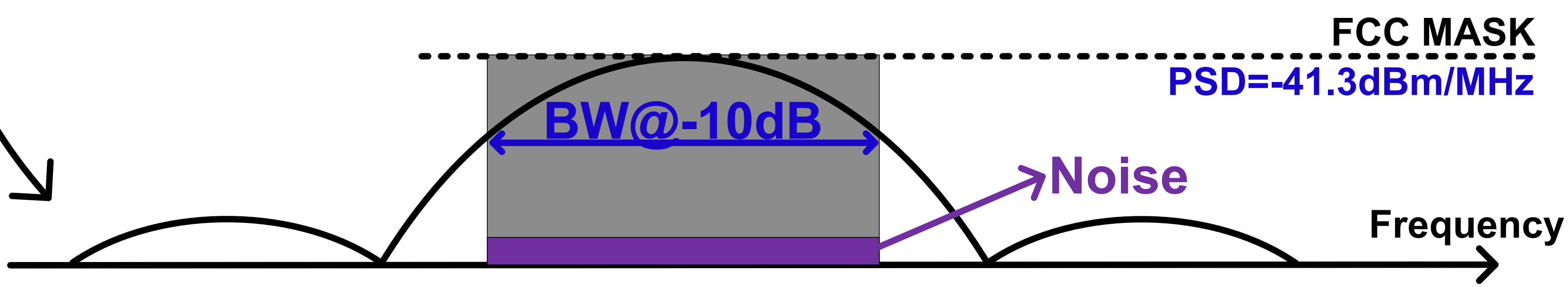
Transmission Power in IR-UWB



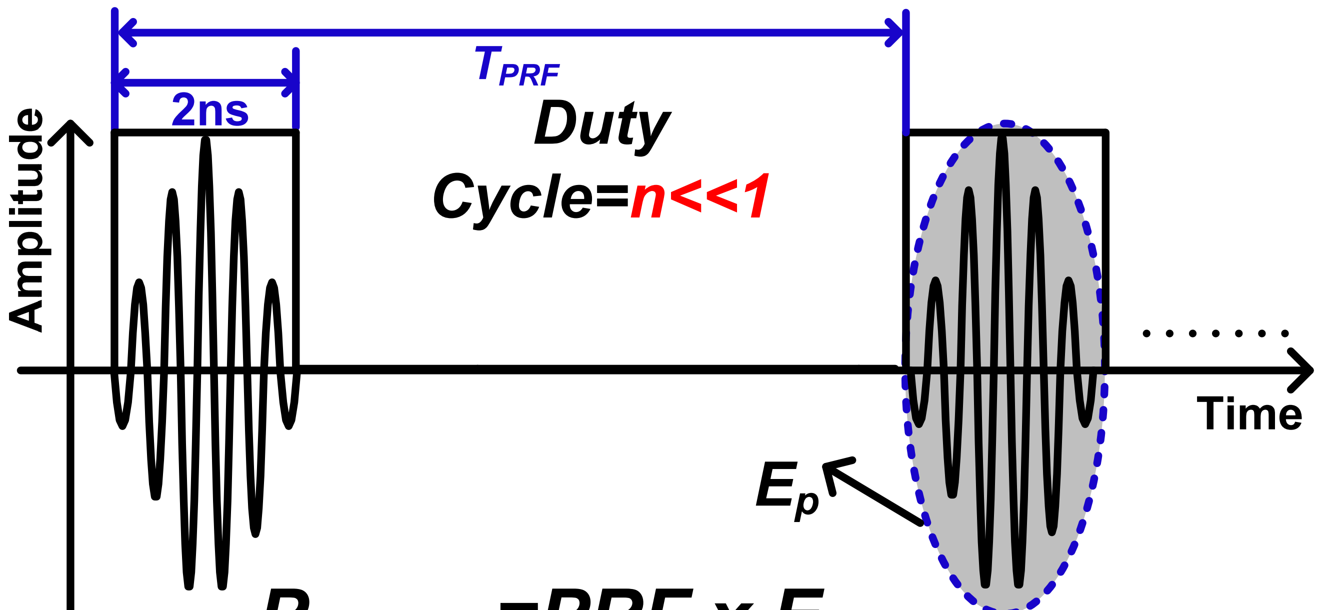
Duty Cycle: T_{pulse}/T_{PRF}
***PRF**:**P**ulse **R**epetition **F**requency*

$$PRF \times E_p = P_{TX} = PSD \times BW$$

=Maximum Transmission Power !



Link Margin in Non-coherent IR-UWB

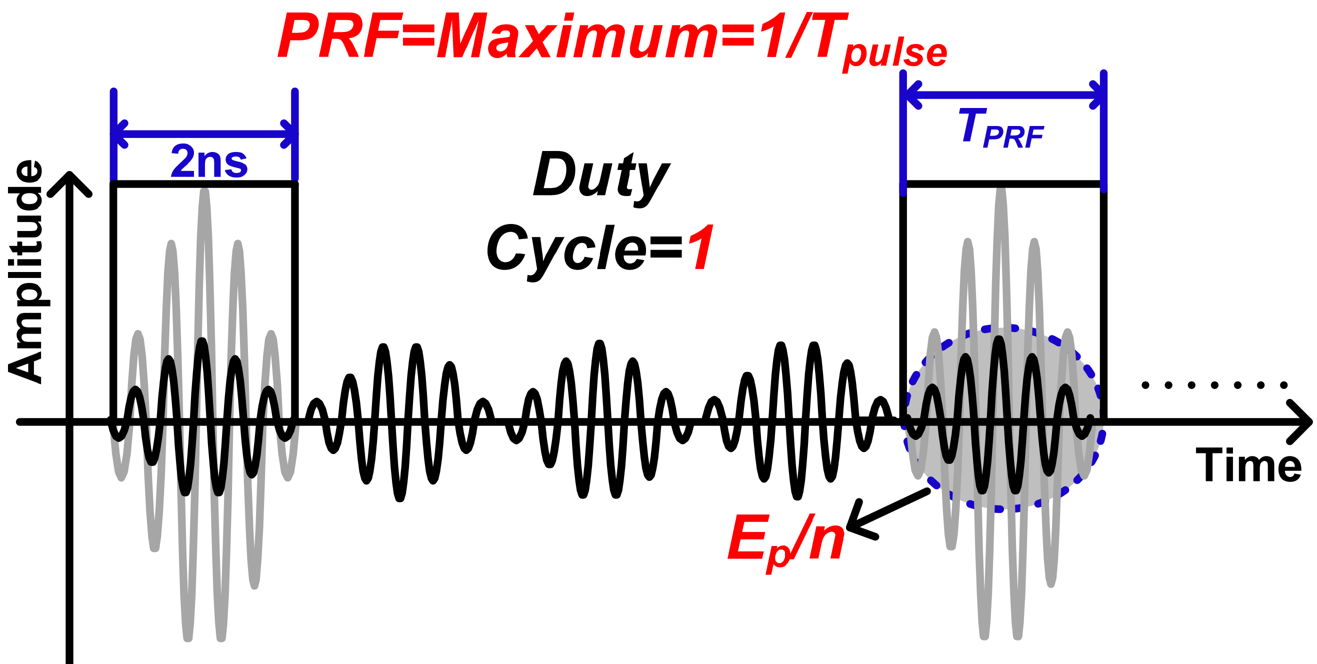


$$P_{TX,MAX} = PRF \times E_p$$

$$SNR_{RX} = E_p \times Loss_{path} / Noise$$

- LM enhanced by increased *SNR* of each pulse
- $P_{TX,MAX}$ with low *PRF* can be limited by supply voltage

Limited LM for HDR IR-UWB



$$P_{TX,MAX}=(n)PRF \times (1/n)E_p$$

$$SNR_{RX}= (1/n)E_p \times Loss_{path} /Noise$$

PRF ↑ → E_p ↓ → SNR_{RX} ↓ → Link Margin ↓

How to increase LM for HDR?

$$P_{TX}\uparrow = PSD + 10\log(BW\uparrow)$$

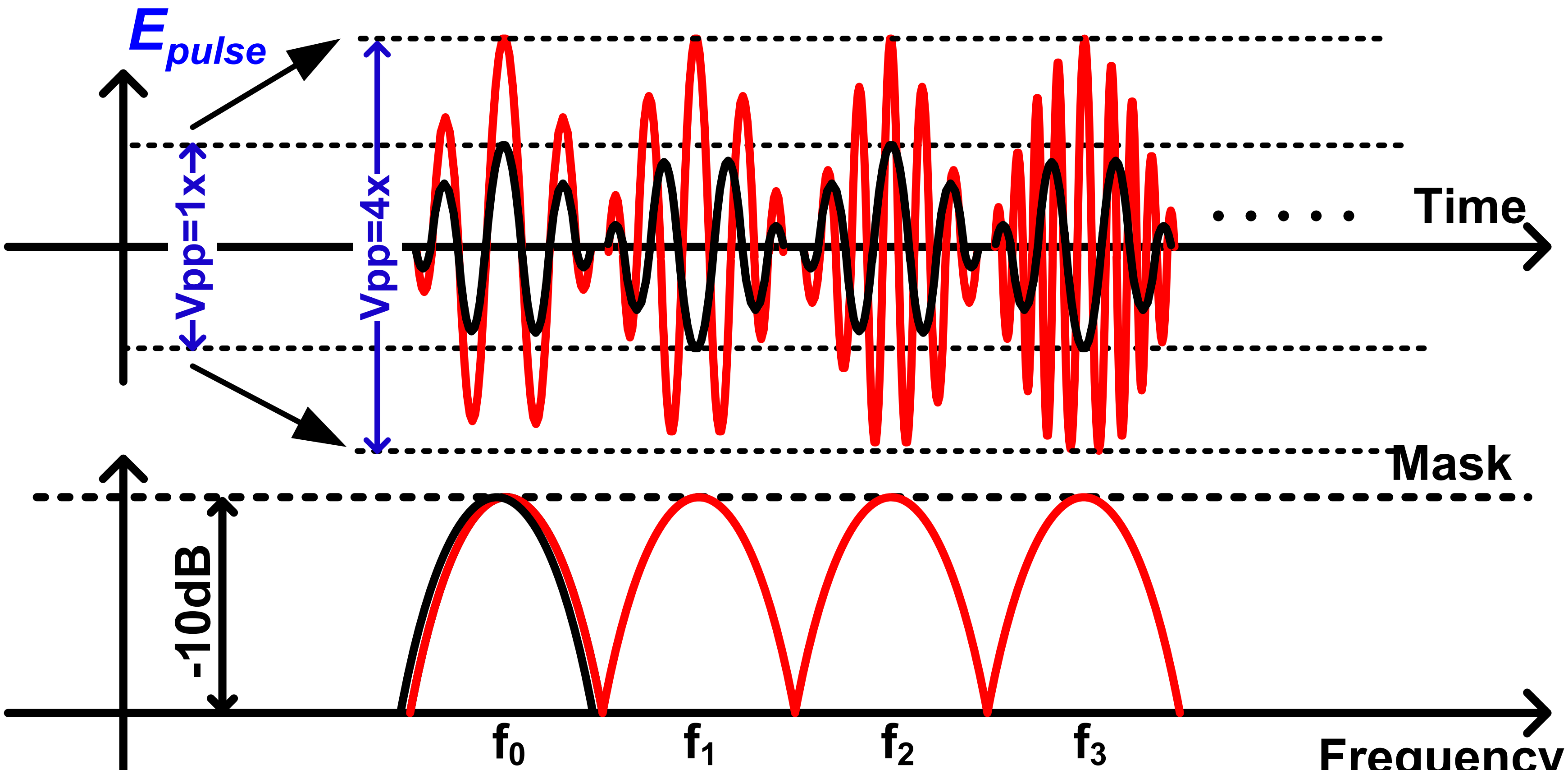
DR/Mbps	Pulse BW/MHz	TX Output Power	Noise Power	*SNR (Receiver)*	Link Margin
500	*500*	P_{TX}	1x	1x	1x
500	*1000*	$2P_{TX}$	2x	1x	1x
500	*2000*	$4P_{TX}$	4x	1x	1x

$P_{TX}=P_{MAX}=-41.3dBm/MHz+10log(500MHz)$
Assume the same NF and required E_b/N_0 for OOK in RX

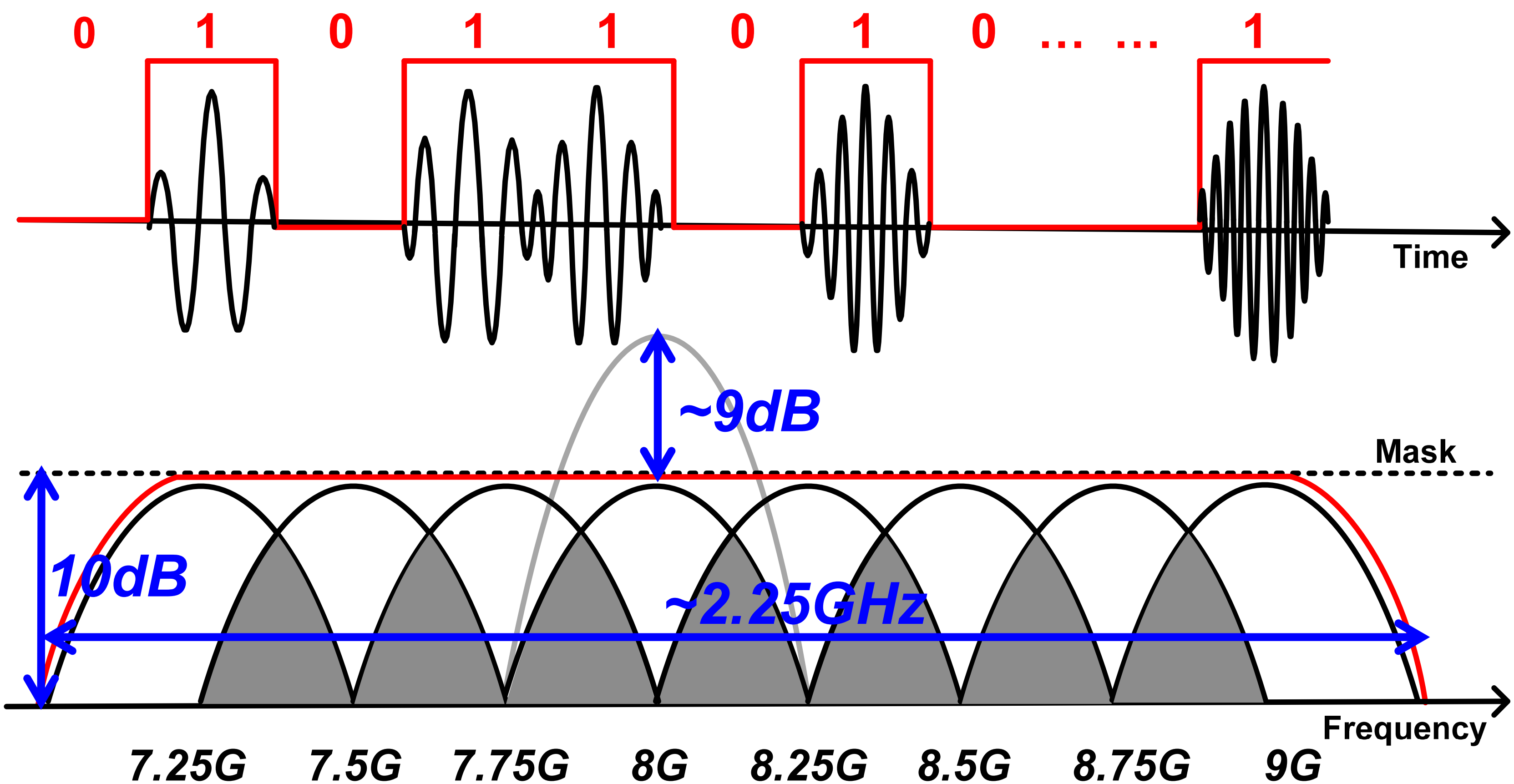
- Increasing pulse bandwidth cannot improve the link margin for HDR transmission

Proposed Solution

- Increase E_{pulse} w/o violating spectrum mask
  → Frequency Hopping (FH) with multiple bands in TX and single band in RX

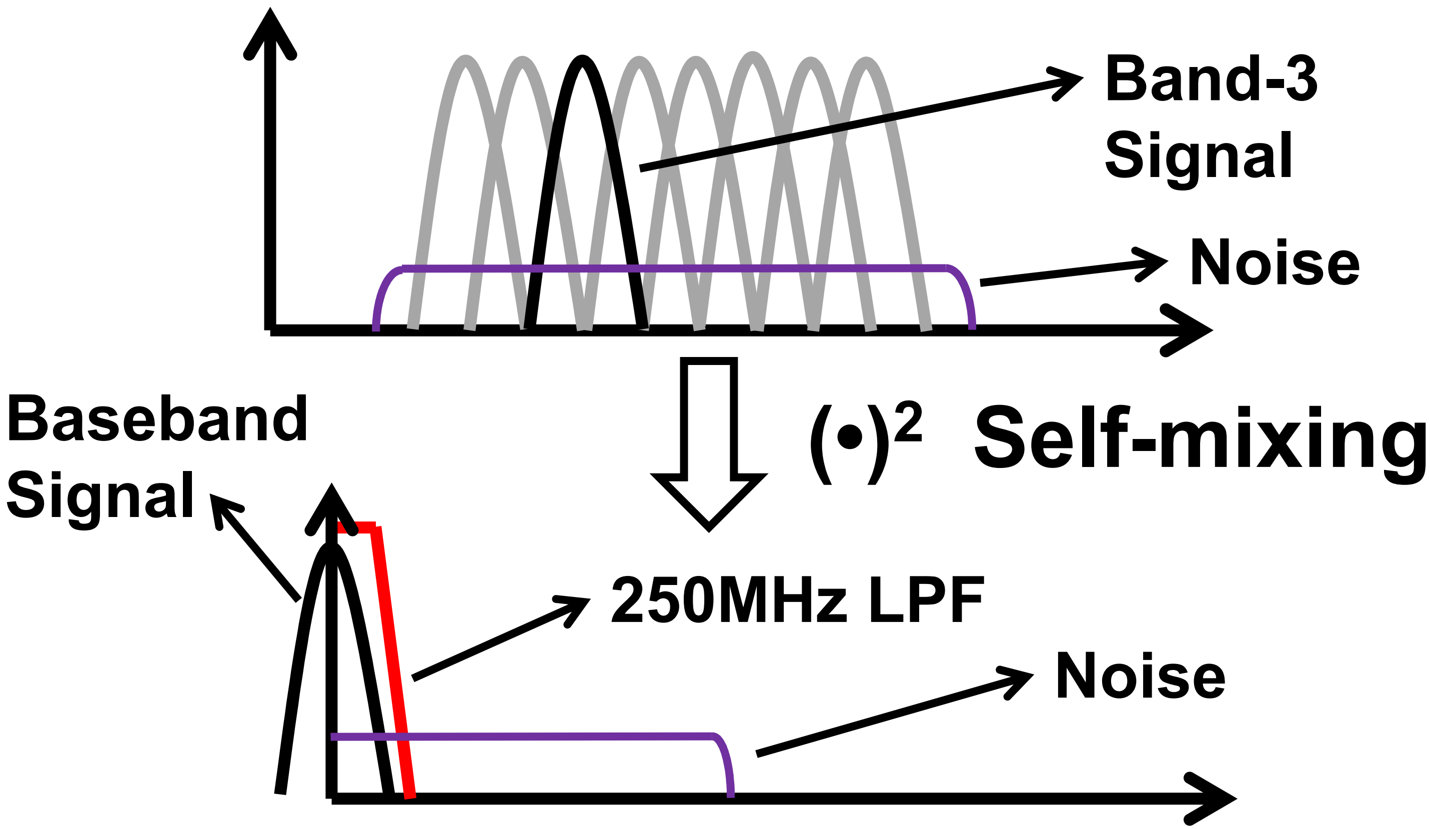


BW Reduction with Overlapped FH



- 50% overlap → Compact spectrum and sharp roll-off
- 8 x 500MHz sub-bands → 2.25 GHz bandwidth

SNR Improvement in Receiver



- Multi-band signals converted to baseband by squarer
- Fixed baseband bandwidth of 250MHz

Overlapped FH

- ✓ OFDM-like sub-bands with 50% overlap
  → >40% overall bandwidth reduction
- ✓ Decouple E_{pulse} from PRF
  → Enhanced link margin with increased E_{pulse}
- ✓ Reduced noise bandwidth at baseband
  → Enhanced SNR in receiver

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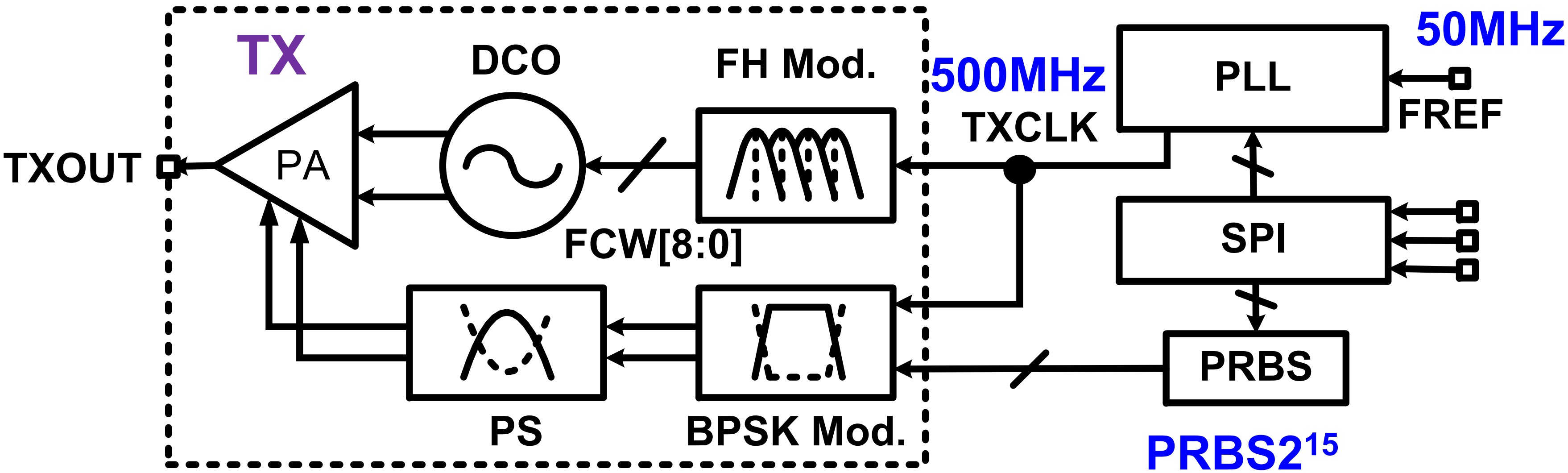
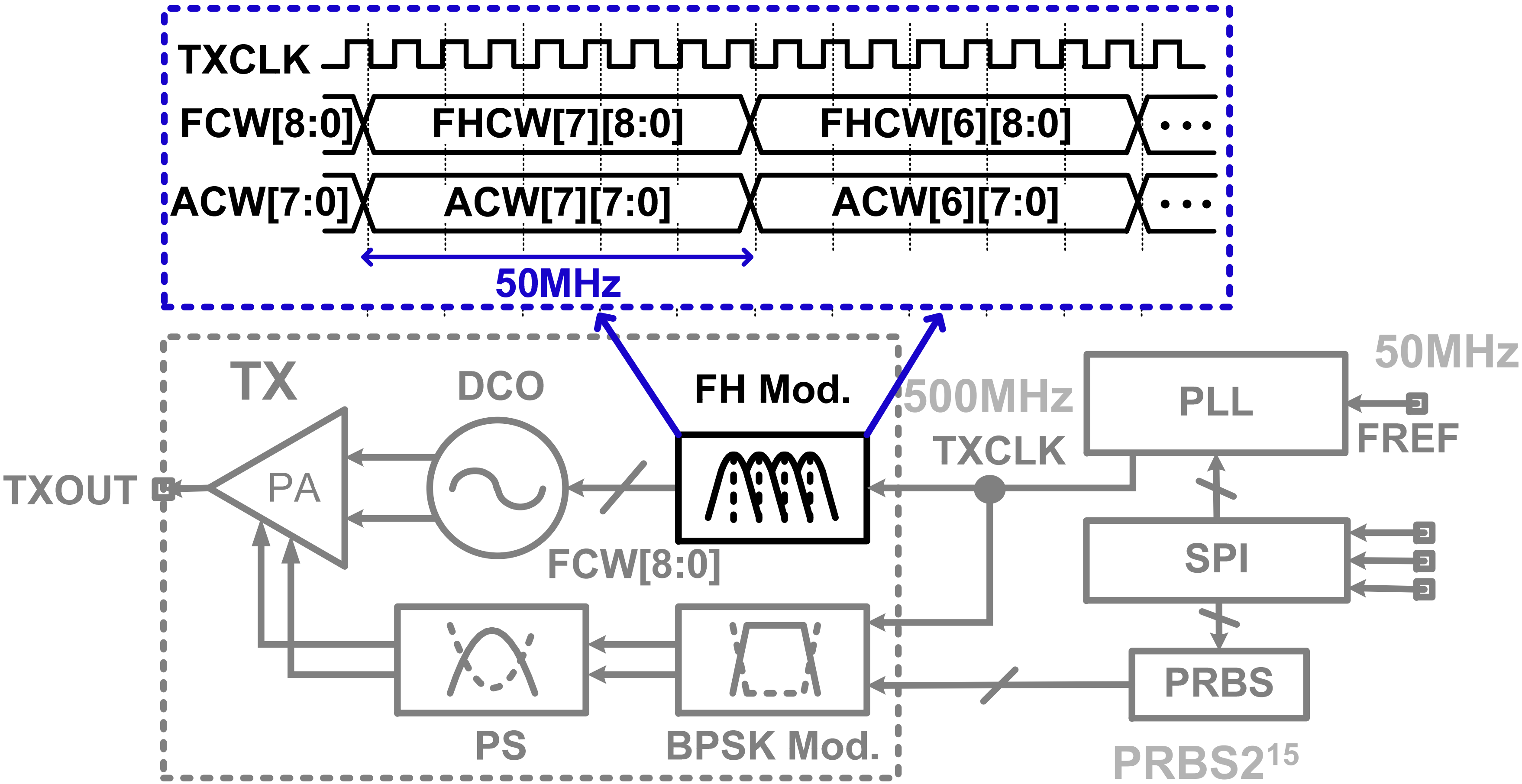
Transmitter Block Diagram

- On-chip integer-N PLL generates 500MHz baseband clock



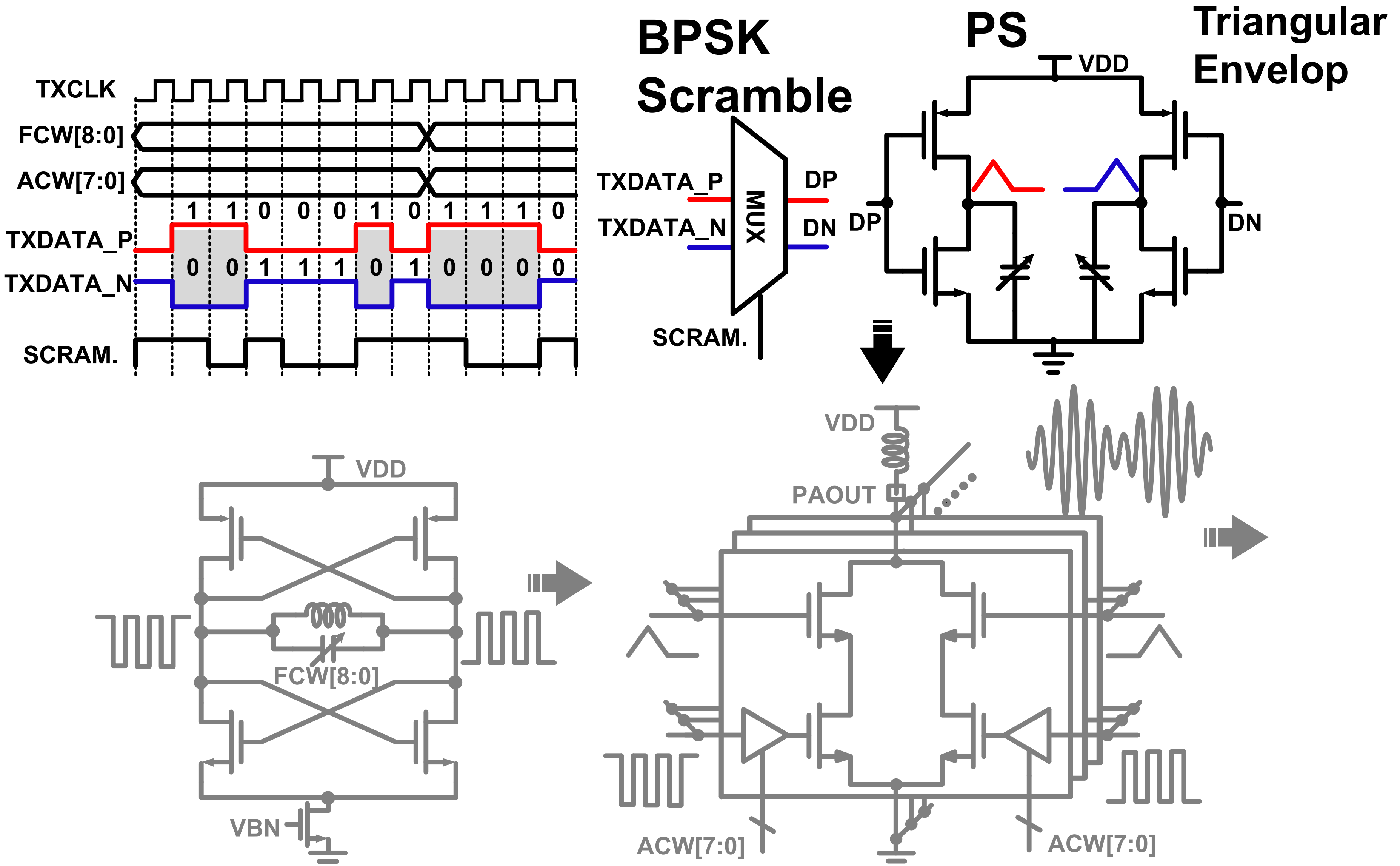
- Open-loop DCO for fast frequency hopping
- Frequency Hopping at 50MHz

Transmitter Block Diagram



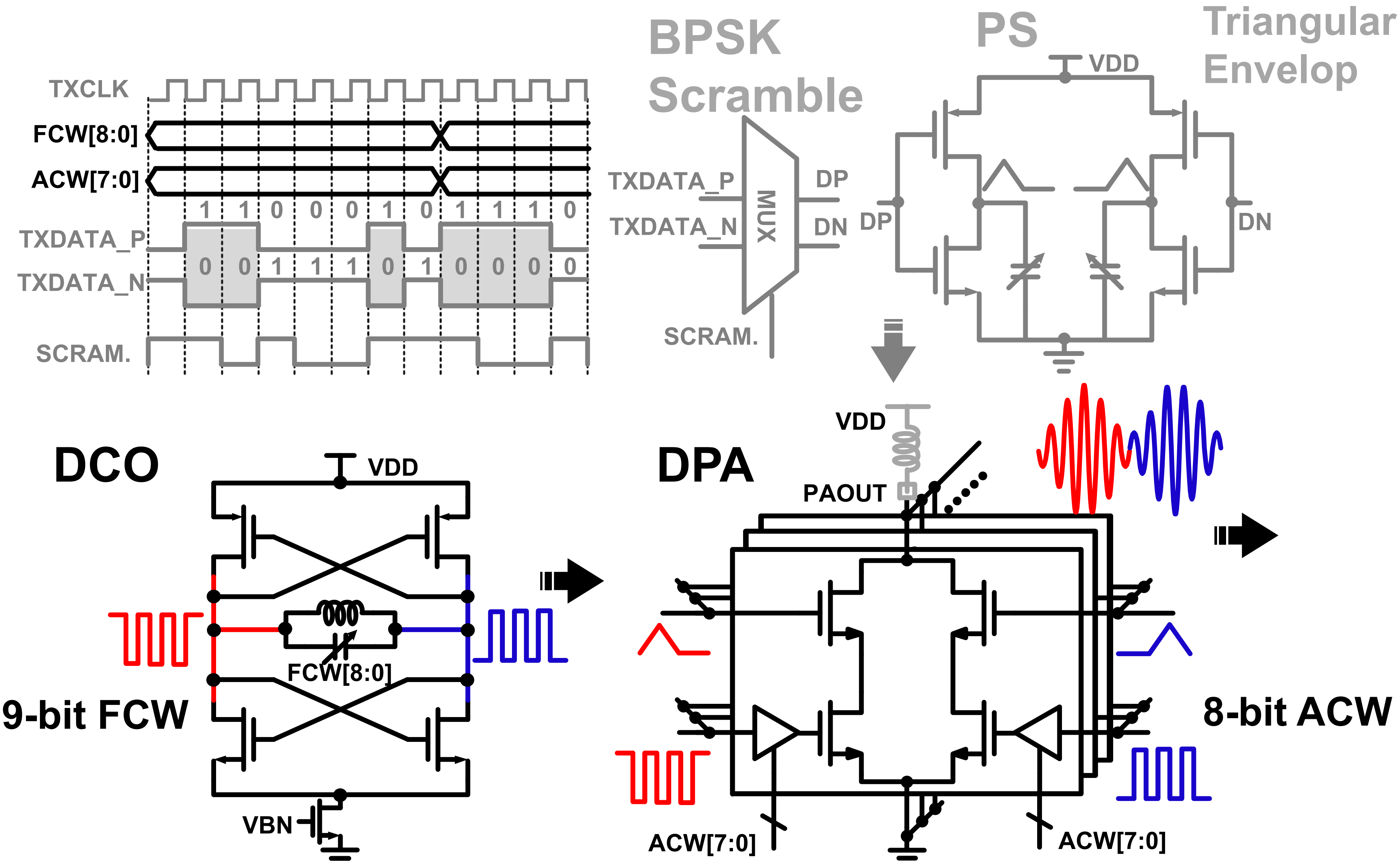
- Open-loop DCO for fast frequency hopping
- Frequency Hopping at 50MHz

DCO/PS/PA



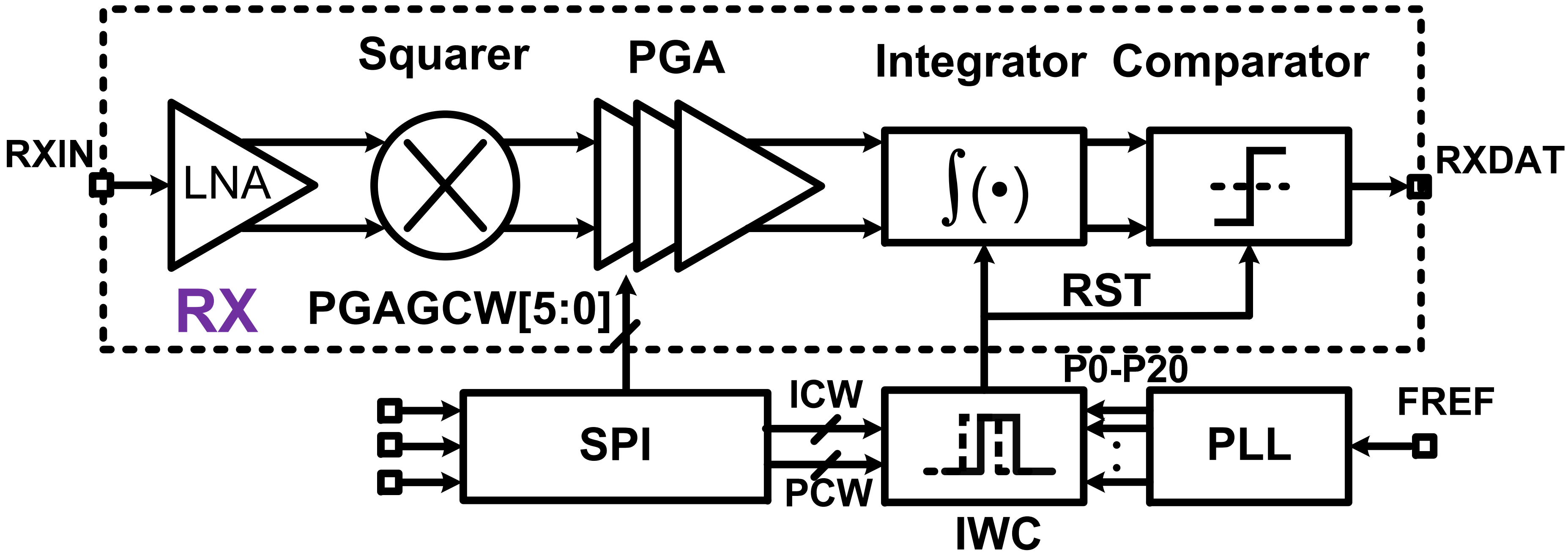
BPSK
Scramble
PS
Triangular
Envelop
TXCLK
FCW[8:0]
ACW[7:0]
TXDATA_P
TXDATA_N
SCRAM.
1 1 0 0 0 1 0 1 1 1 0
0 0 1 1 1 0 1 0 0 0 0
TXDATA_P
TXDATA_N
MUX
DP
DN
SCRAM.
VDD
DP
DN
VDD
FCW[8:0]
VBN
VDD
PAOUT
ACW[7:0]
ACW[7:0]

DCO/PS/PA



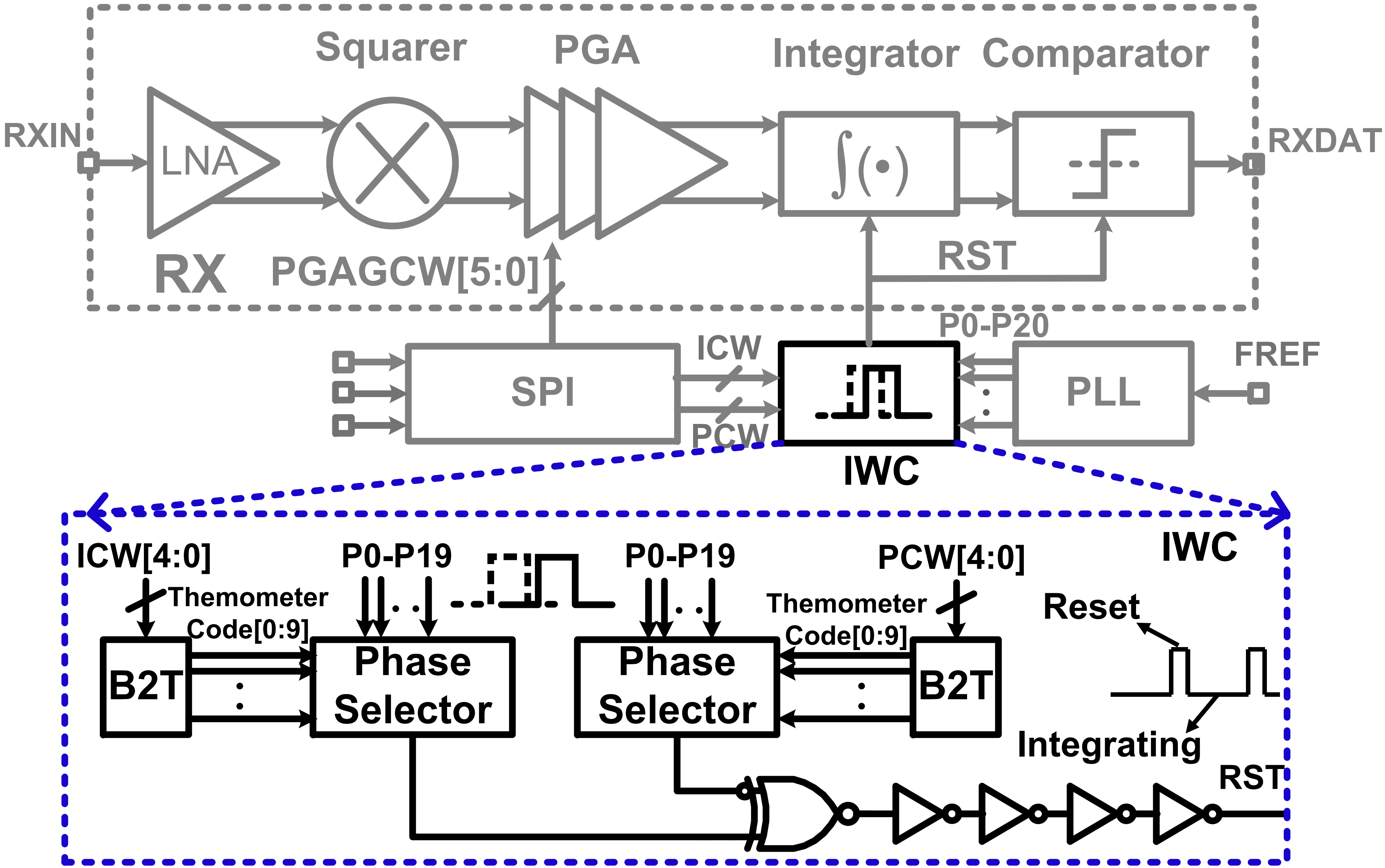
TXCLK
FCW[8:0]
ACW[7:0]
1 1 0 0 0 1 0 1 1 1 0
TXDATA_P
0 0 1 1 1 0 1 0 0 0 0
TXDATA_N
SCRAM.
BPSK Scramble
TXDATA_P
TXDATA_N
MUX
DP
DN
SCRAM.
PS
VDD
DP
DN
Triangular Envelop
DCO
VDD
FCW[8:0]
9-bit FCW
VBN
DPA
VDD
PAOUT
8-bit ACW
ACW[7:0]
ACW[7:0]

Receiver Block Diagram

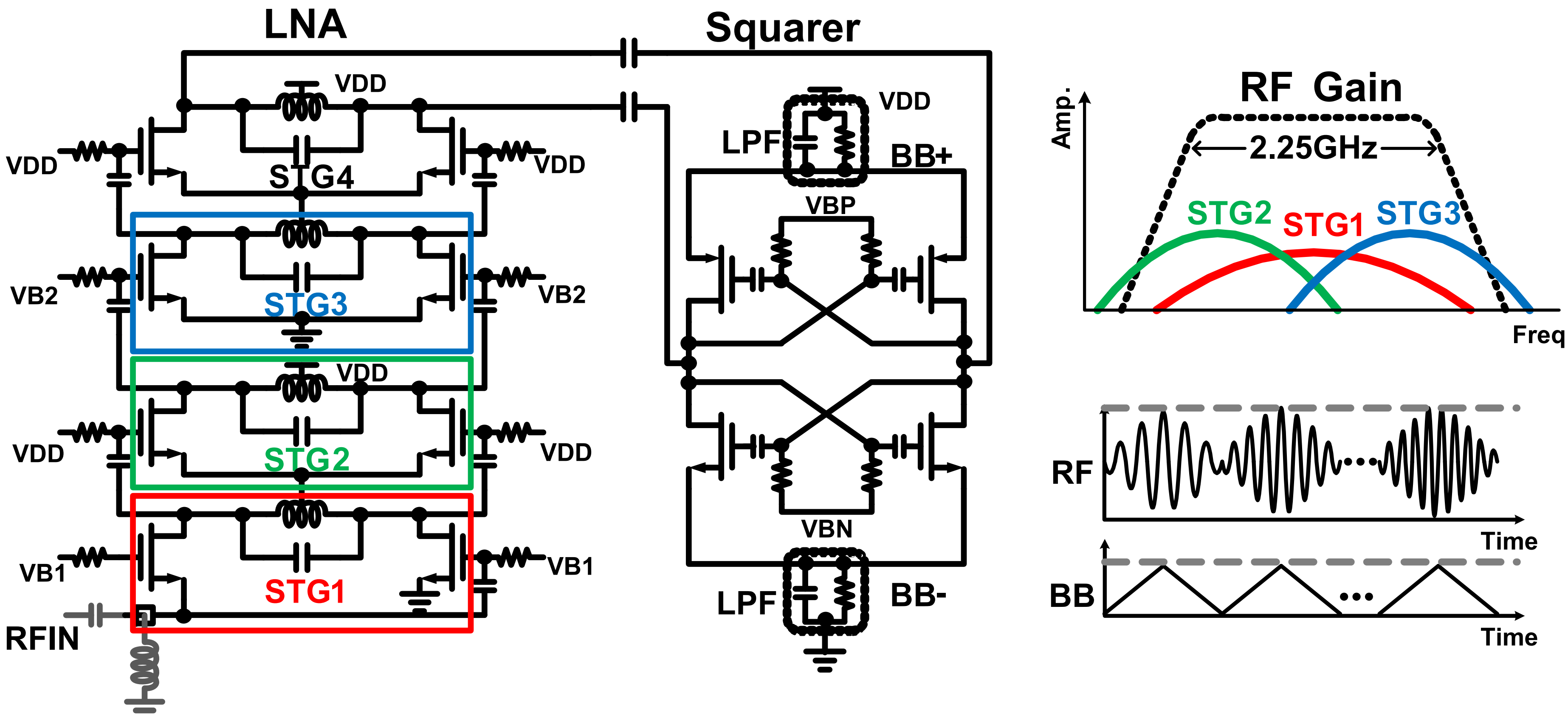


- Typical energy detector based IR-UWB receiver
- Symbol-level synchronization manually tuned by 5-bit phase control word(PCW)
- Optimized integrating window manually tuned by 5-bit integrating control word(ICW)

Receiver Block Diagram

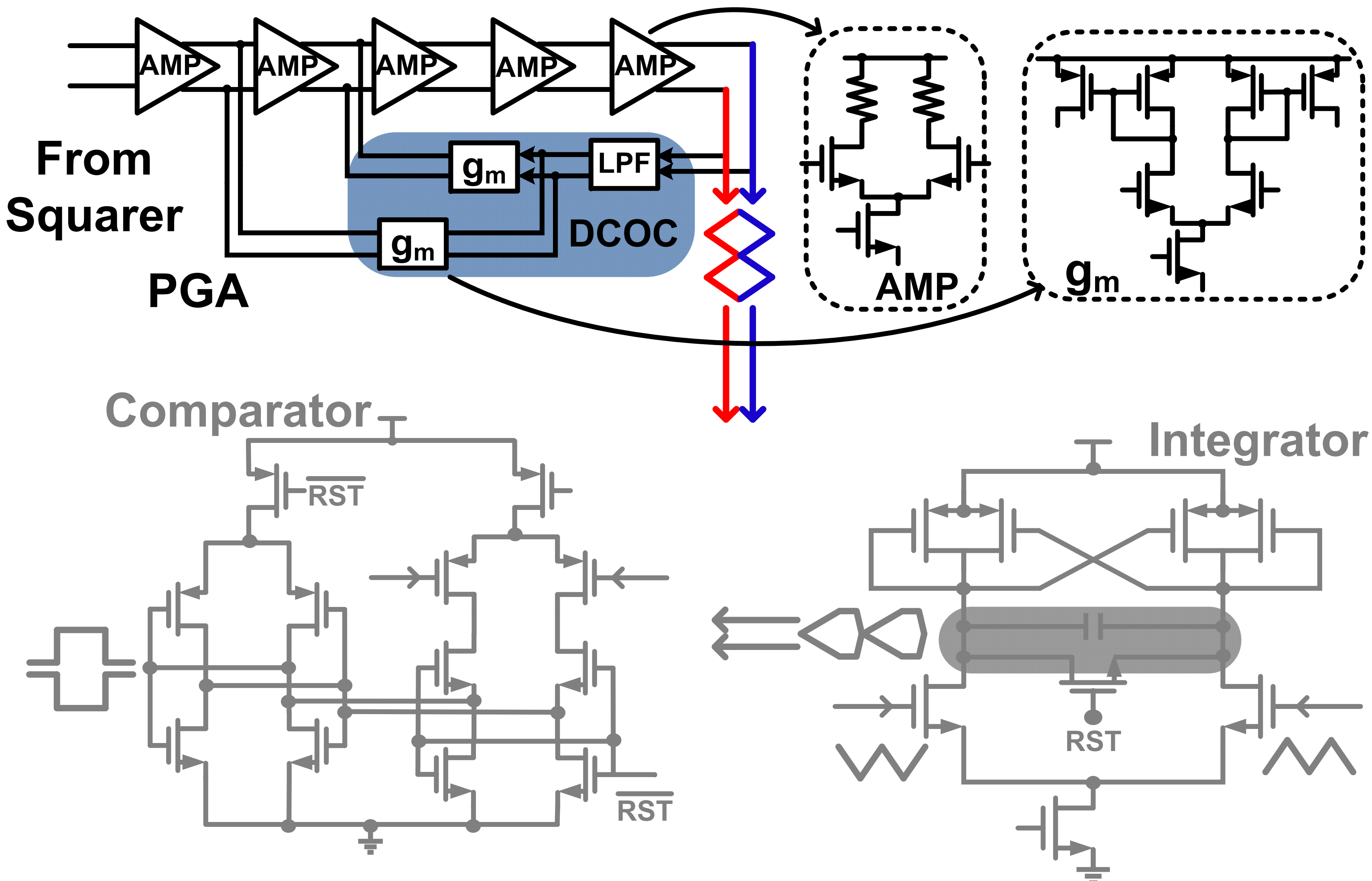


LNA/Squarer

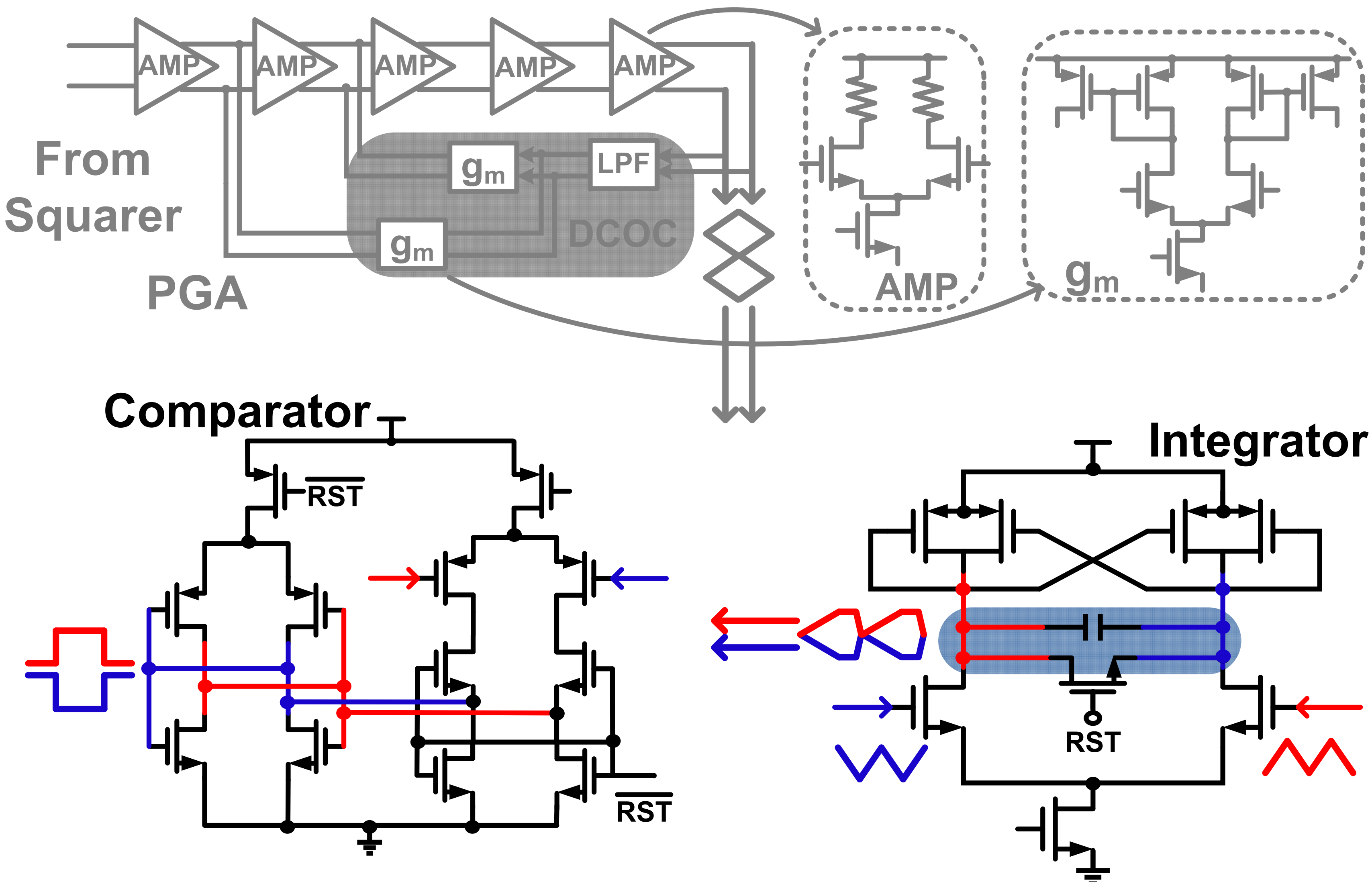


- Balun-combined current-reuse stacked LNA
- 2.25GHz BW with three combined stages

PGA/Integrator/Comparator



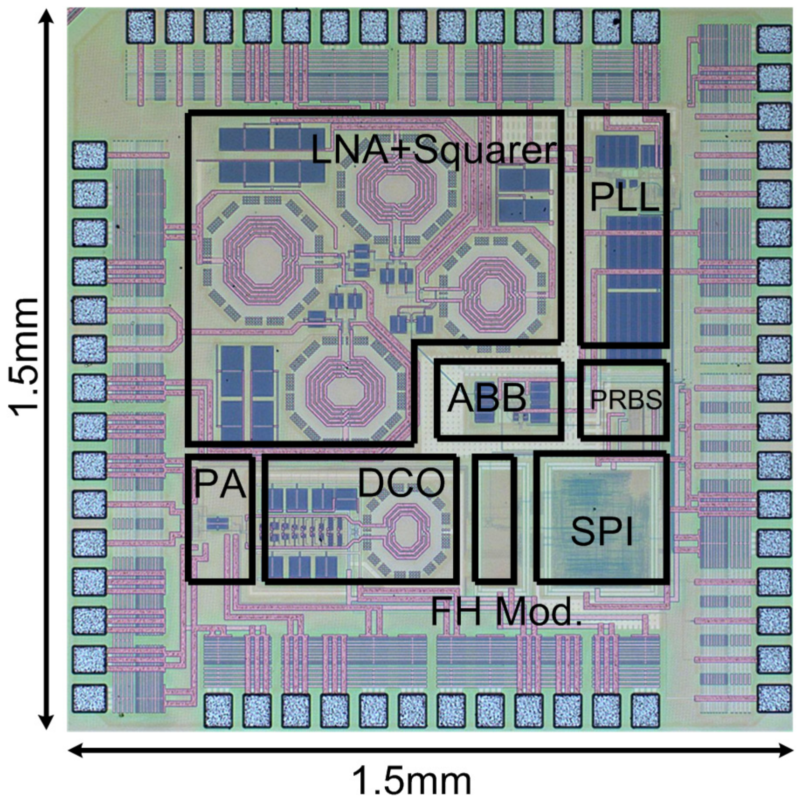
PGA/Integrator/Comparator



Outline

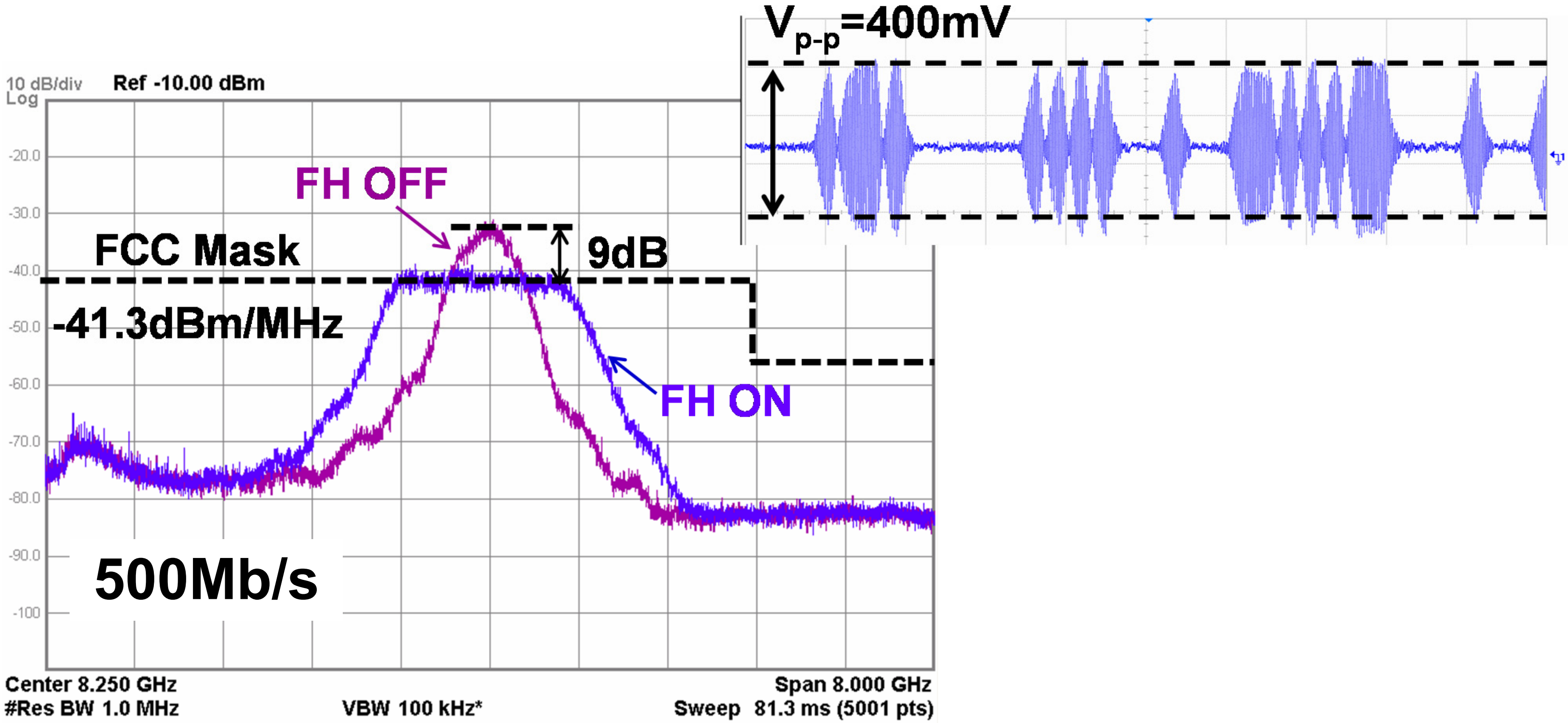
- Introduction
- System Design
  - HDR transmission in IR-UWB
  - Enhanced link margin with FH
- Implementation
- **Measurement Results**
- Summary

Chip Micrograph



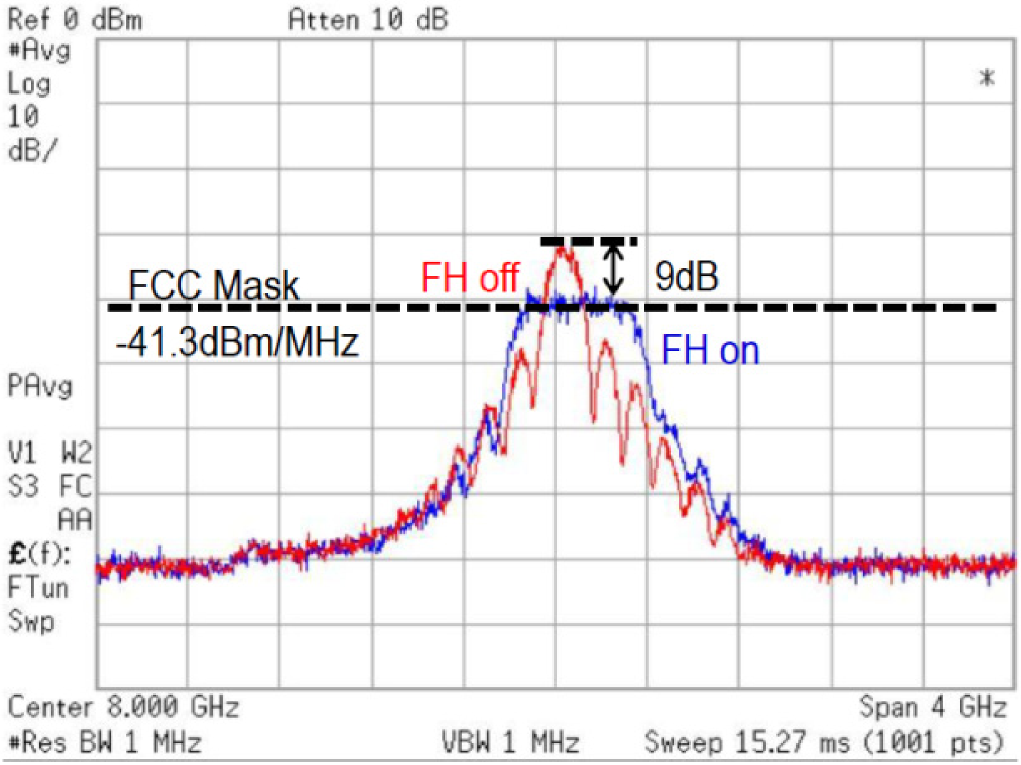
- Fabricated in 65nm CMOS
- Chip area including PAD: 2.25mm^2
- First meter-range 500Mb/s 26pJ/bit transmission

Measured Transmitter Performance



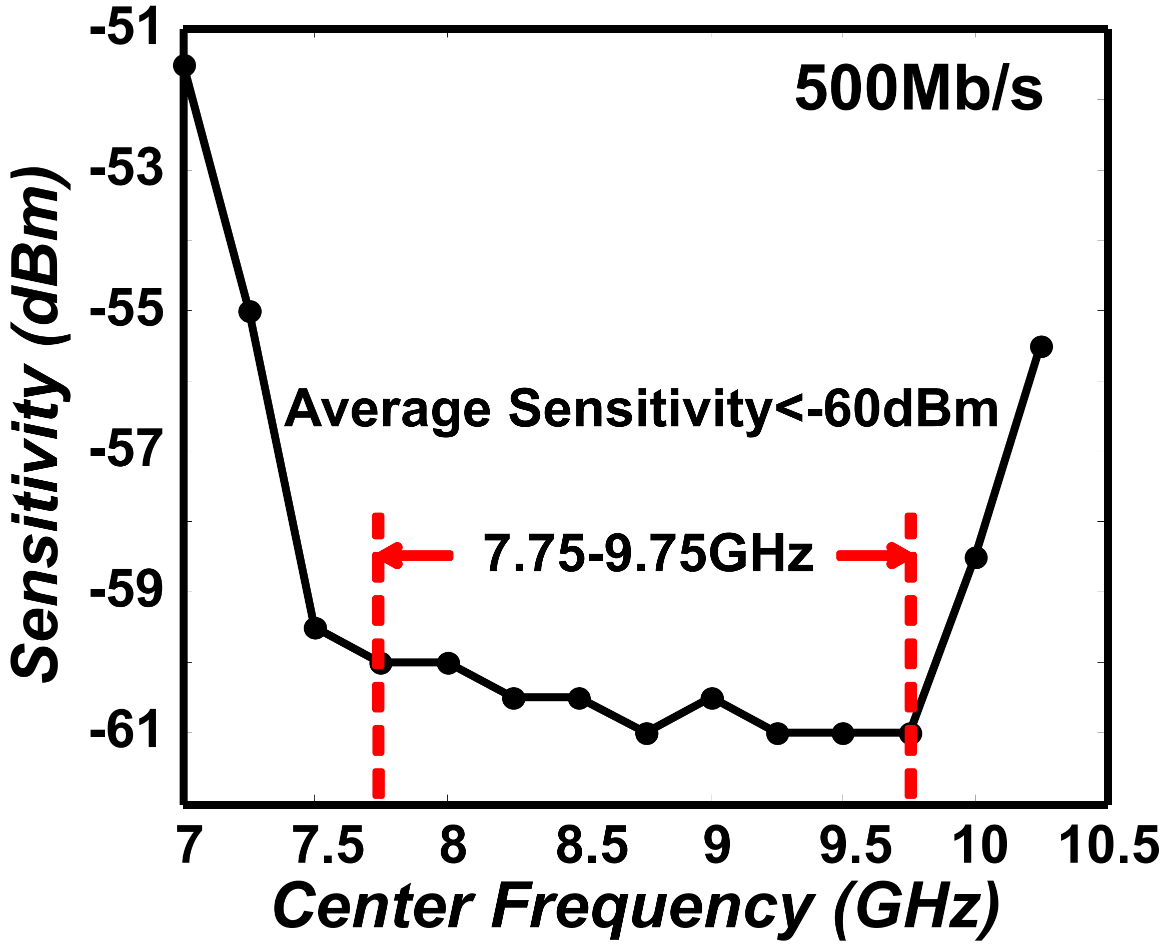
- 2GHz BW with high spectrum efficiency
- Flat spectrum with gain equalization by ACW

Measured Spectrum at 125Mb/s



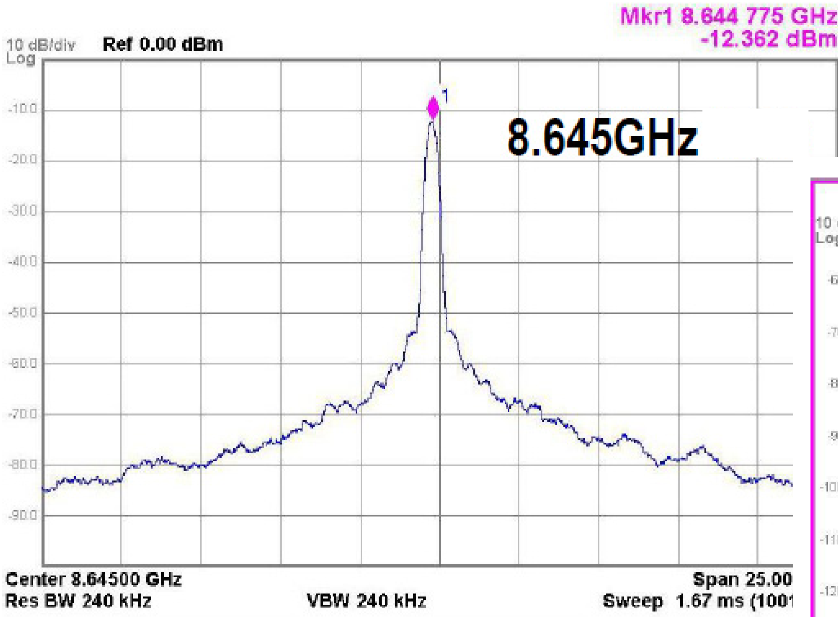
- 500MHz overall BW (8 x 125MHz, 50% overlap)
- Steeper spectral roll-off than conventional UWB
  → Proposed method can be generalized for any DR

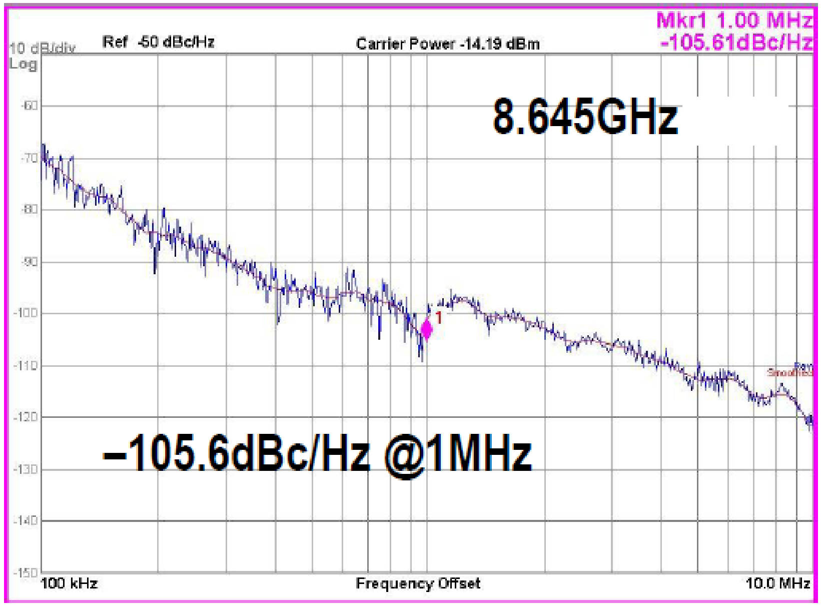
Measured Receiver Sensitivity



- Sensitivity of <-60dBm over 7.75-9.75GHz

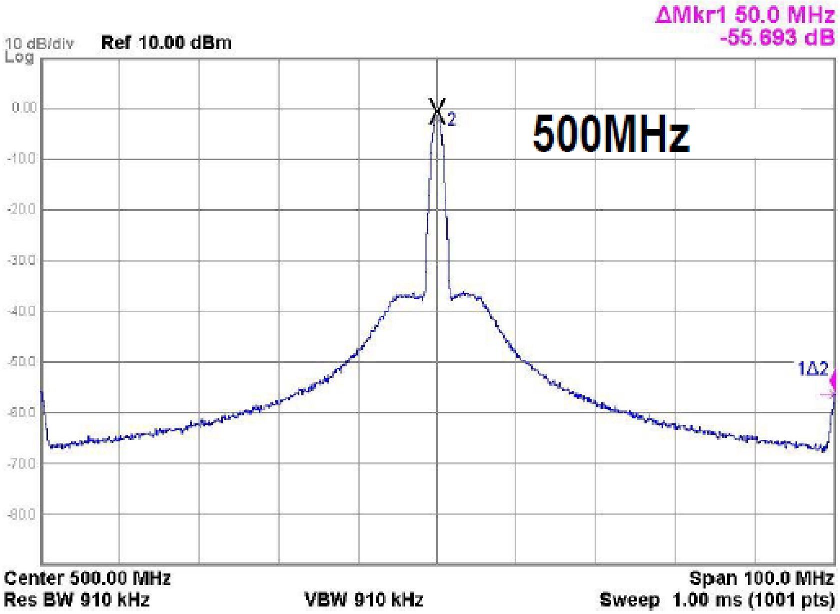
Measured DCO Performance

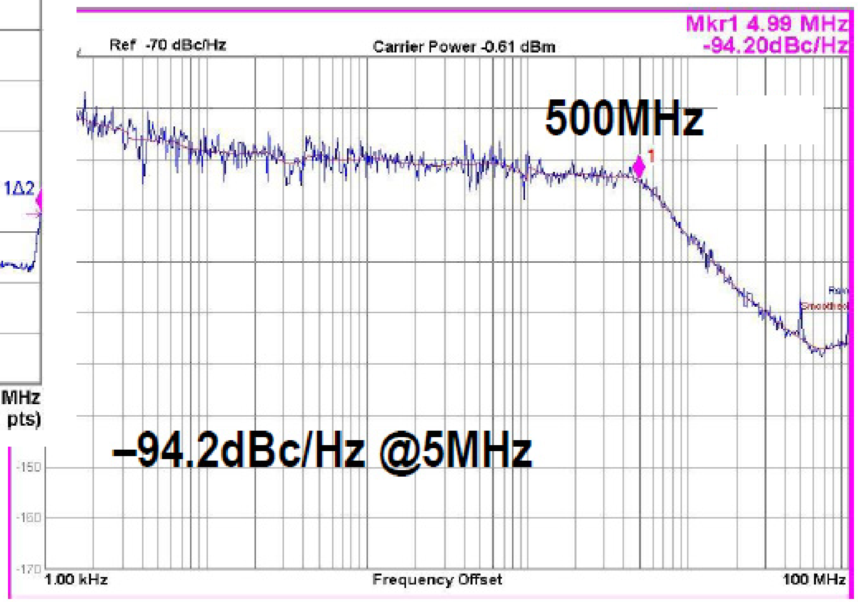




- 7.4-10.3GHz tuning range, -105dBc/Hz@1MHz offset
- 2.26mW power consumption

Measured PLL Performance

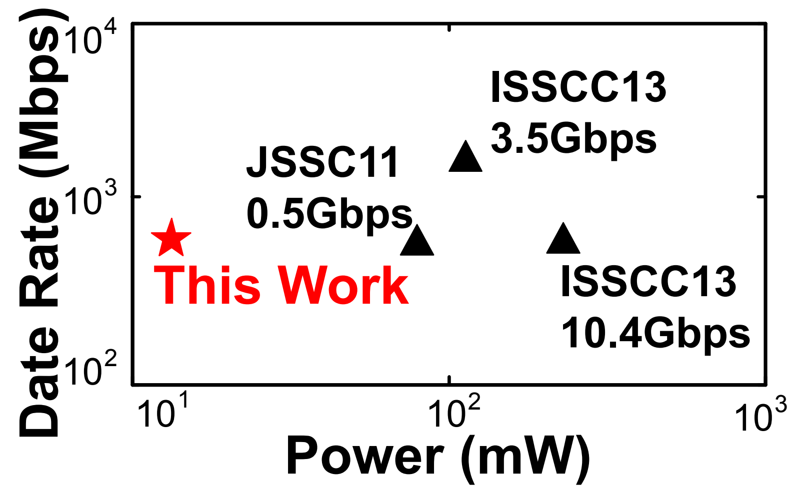


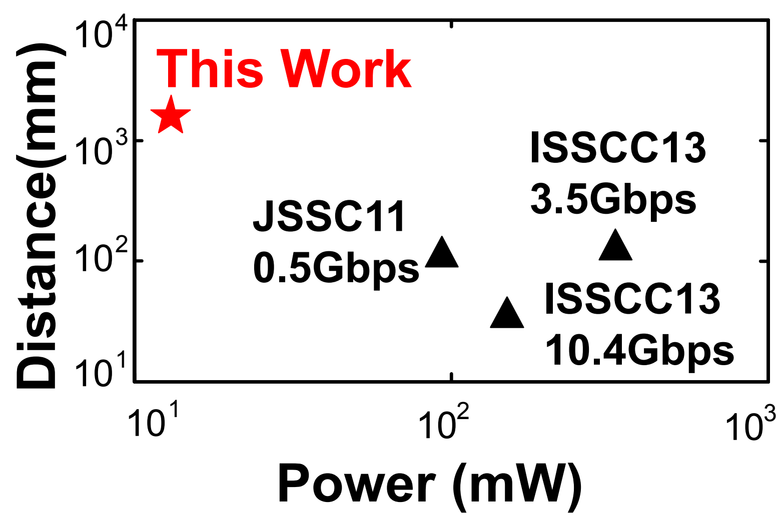


- 300-700MHz locking range, 0.5mW power
- -56dBc ref. spur @50MHz, -94dBc/Hz @5MHz

Performance Summary

	This Work
RF Band	7.5-9.5GHz
Modulation	OOK
Data Rate	125-500Mb/s
Power Consumption	13.3mW @500Mb/s (TX: 6.9mW, RX: 5.9mW, PLL: 0.5mW)
Communication Distance	0.4m (without FH) >1.2m (with FH)
TX Output Power	-7.5dBm @500Mb/s
RX Sensitivity	-60dBm @500Mb/s
Process	65nm CMOS





Outline

- Introduction
- System Design
  - HDR transmission in IR-UWB
  - Enhanced link margin with FH
- Implementation
- Measurement Results
- **Summary**

Summary

- 13mW 500Mb/s meter-range transceiver implemented in 65nm CMOS
  - Overlapped FH for enhanced link margin
  - High energy efficiency of 26pJ/bit
- Feasibility of >3m range HDR transmission with multiple antennas

Acknowledgment

This work was partly supported by Global Research Outreach (GRO) Program of Samsung Advanced Institute of Technology (SAIT), Suwon, Korea.

9.3
A 1mW 1Mb/s 7.75-to-8.25GHz Chirp-UWB Transceiver with Low Peak Power Transmission and Fast Synchronization Capability

Fei Chen[1], Yu Li[1], Dang Liu[1], Woogeun Rhee[1], Jongjin Kim[2], Dongwook Kim[2], and Zhihua Wang[1]

[1]Tsinghua University, Beijing, China;
[2]Samsung Advanced Institute of Technology, Suwon, Korea

清华大学微电子学研究所
Institute of Microelectronics, Tsinghua University

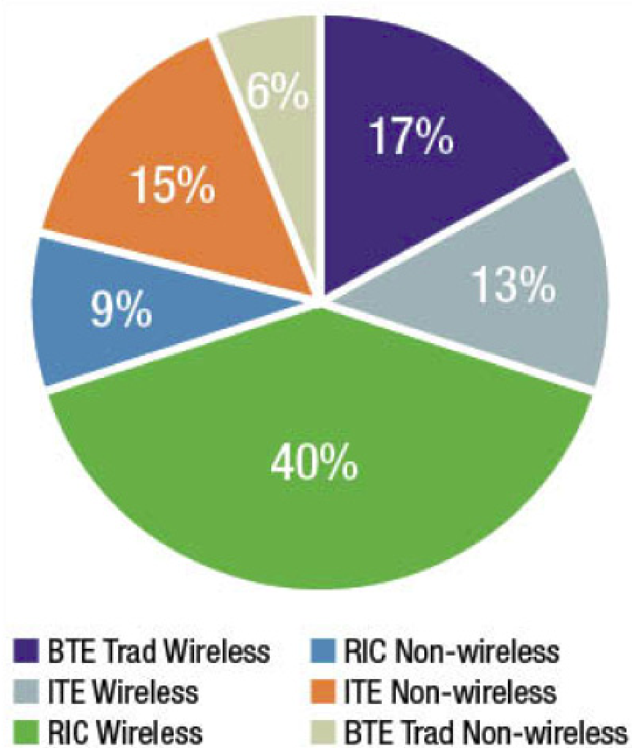
Outline

- Background
- Chirp-UWB Technique
- Transceiver Design
  - – Digital-intensive UWB generation
  - – Double-balanced FM demodulation
- Measurement Results
- Summary

Outline

- **Background**
- Chirp-UWB Technique
- Transceiver Design
  - Digital-intensive UWB generation
  - Double-balanced FM demodulation
- Measurement Results
- Summary

Wireless Hearing Aids



(Ref: K.E. Strom, “Hearing aid sales flat in first quarter; wireless 70% of market,” *Hearing Review*, May 2013)

- BTE (behind the ear)
- ITE (in the ear)
- RIC (receiver in the ear)

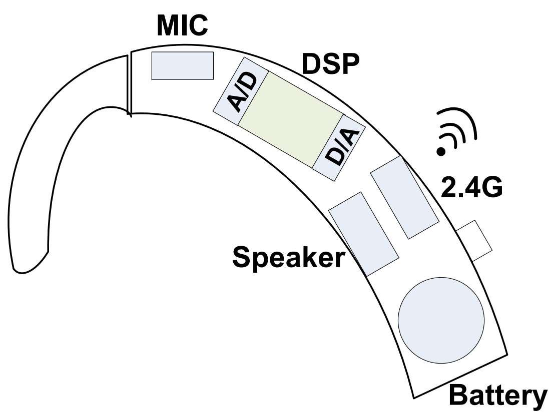
- Hearing aids in high demand in the aging-world
  - **$15 billion for 360 million people** [Reuters, Nov 2013]
- Wireless hearing aids become dominant
  - Fast growing, reaching **70% of the market**

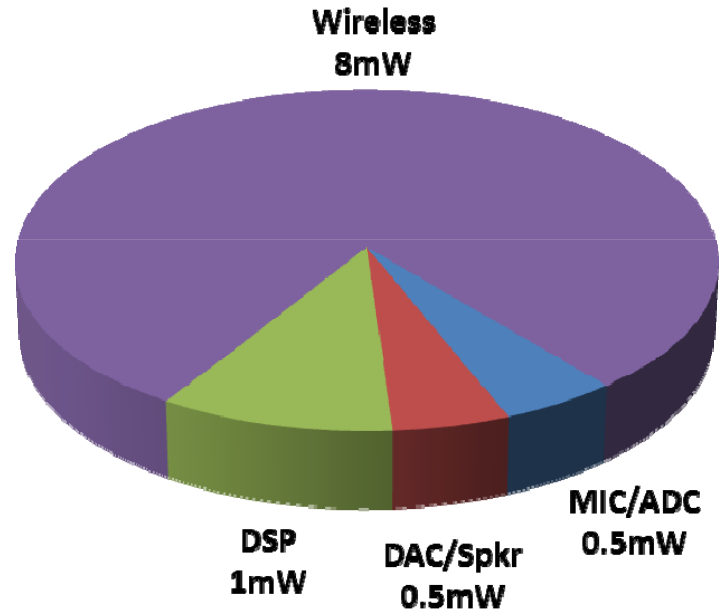
High-Quality Hearing Aids

- Binaural or streaming requires higher data rate.
  - **Ear-to-ear** improves directivity.
  - **Ear-to-audio** connects to TV, smartphone, etc.
- BLE or Bluetooth-like solutions ongoing

Power Consumption is the Key

*source: nuear

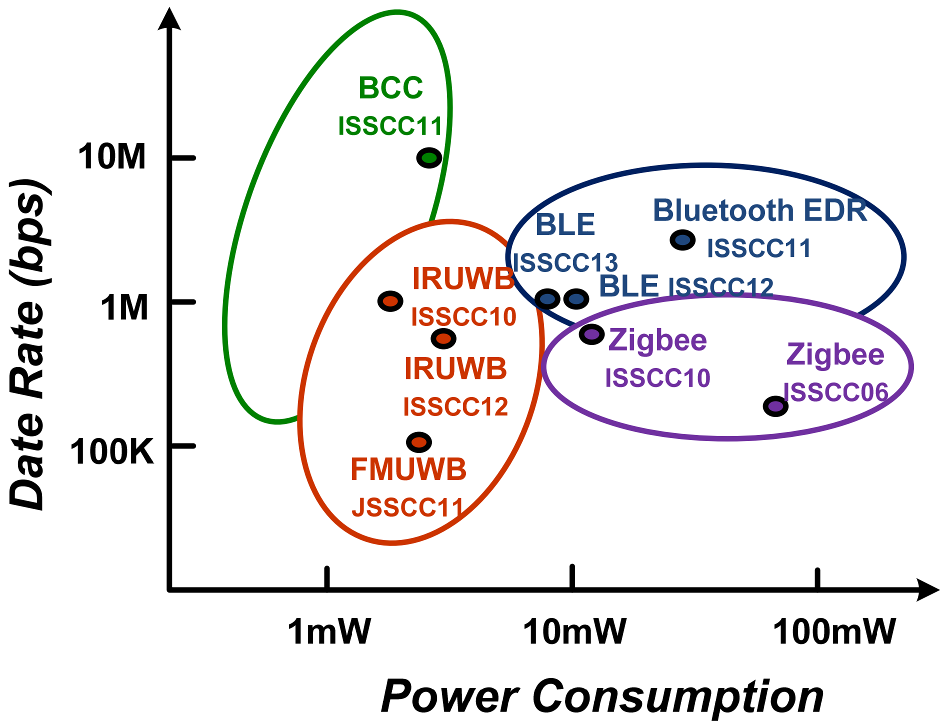


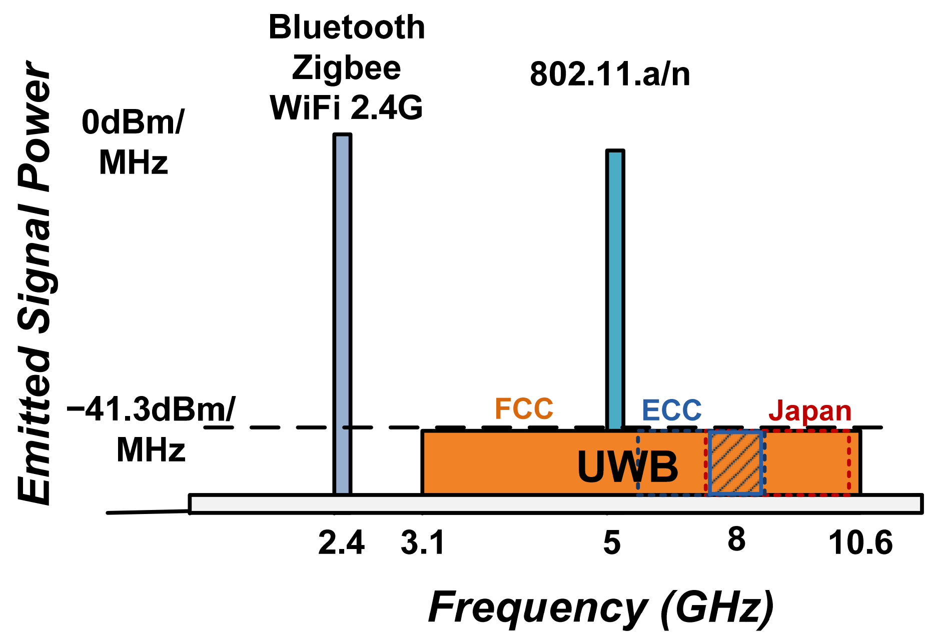


- **>70% power** is consumed by wireless transceiver
- Miniaturized device has **~100mAh** Zinc-Air battery
- BLE or coherent UWB >5mW, 1~2 day/bat.

→ **Sub-mW wireless TRX is desired**, 1 week/bat.

High-Band UWB Transceiver



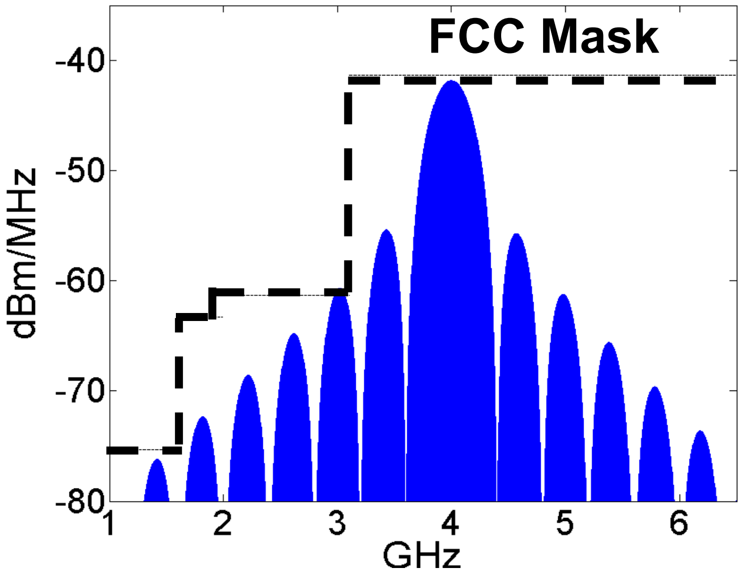


- **High-band UWB** is free from narrowband interference
- **<3m hearing-aid range** limits max number of nearby UWB users and relax RX sensitivity
- Target: **Sub-mW 1Mb/s TRX in 8GHz sub-band**

Outline

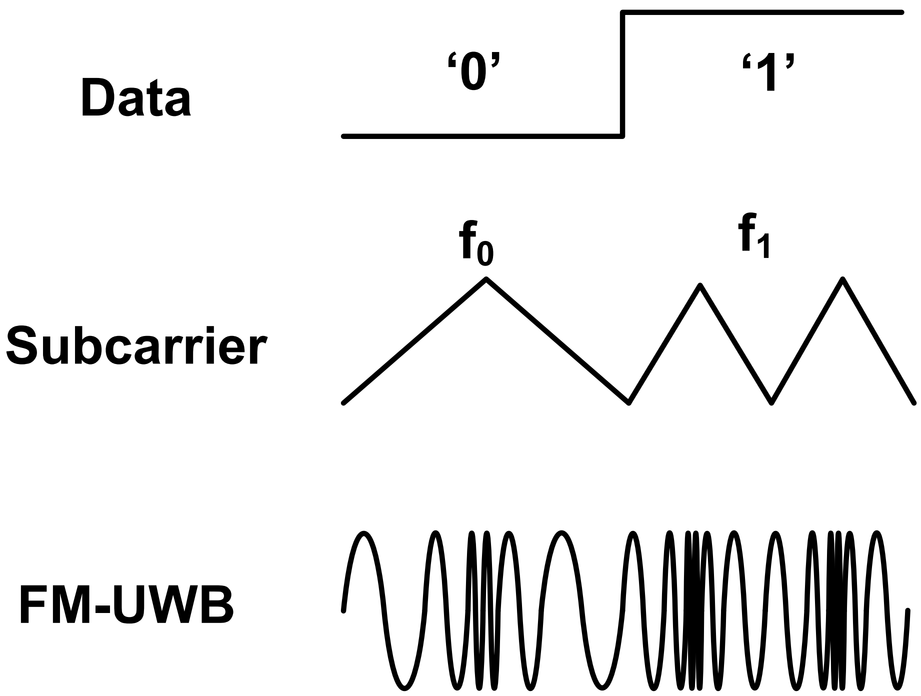
- Background
- **Chirp-UWB Technique**
- Transceiver Design
  - Digital-intensive UWB generation
  - Double-balanced FM demodulation
- Measurement Results
- Summary

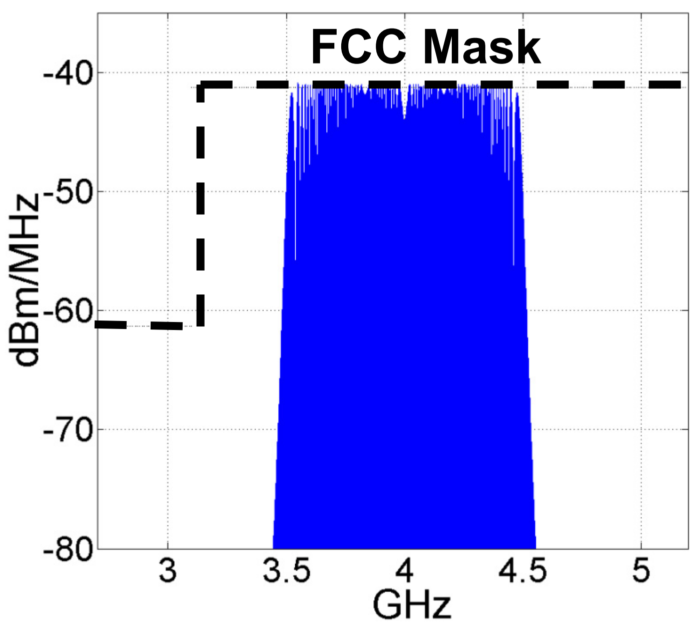
IR-UWB for LDR Applications



- Ultra-low power with **aggressive duty cycle**
- **Complex bit synchronization**
- Very **large peak power** for low data rate
- Difficult to control spectrum bandwidth over PVT

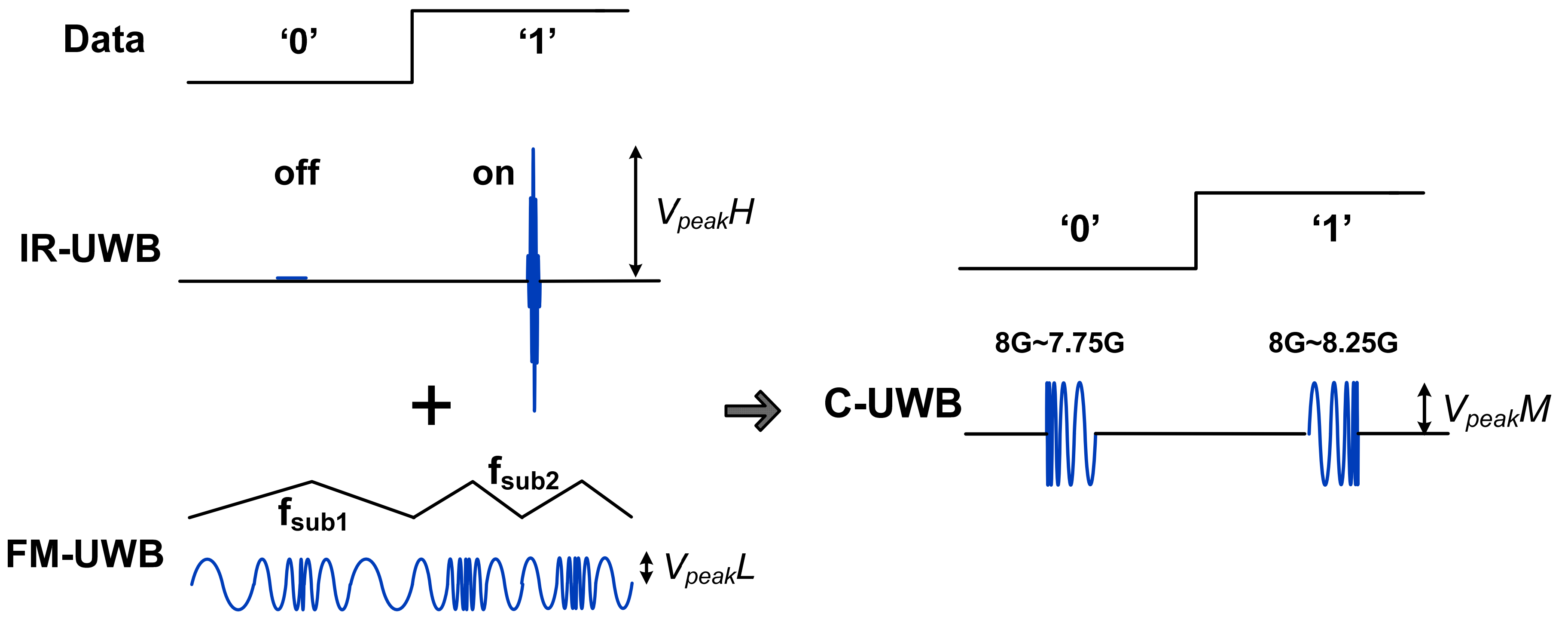
2-FSK FM-UWB





- Constant envelope with **good bandwidth control** with steep spectral roll-off
- **No duty-cycled** operation, so difficult for low-power design

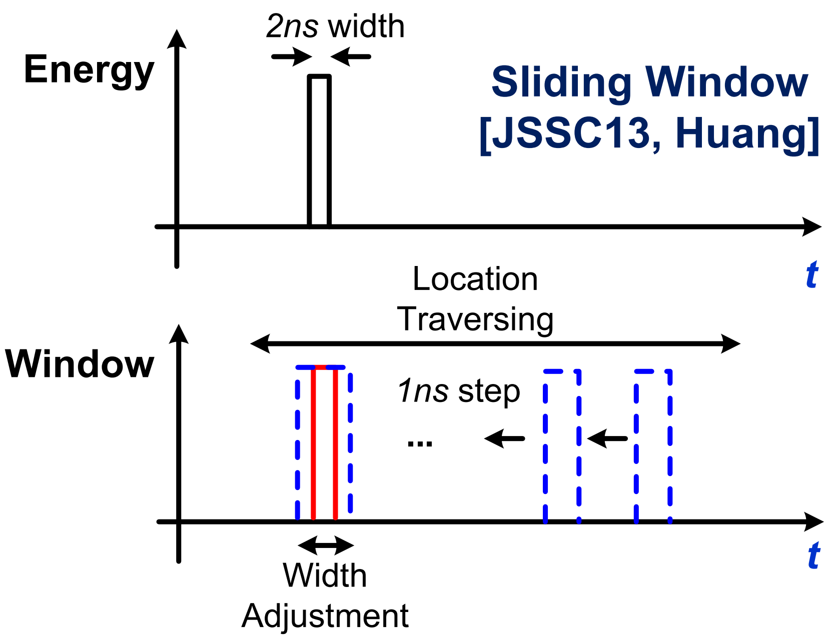
2-FSK Chirp-UWB



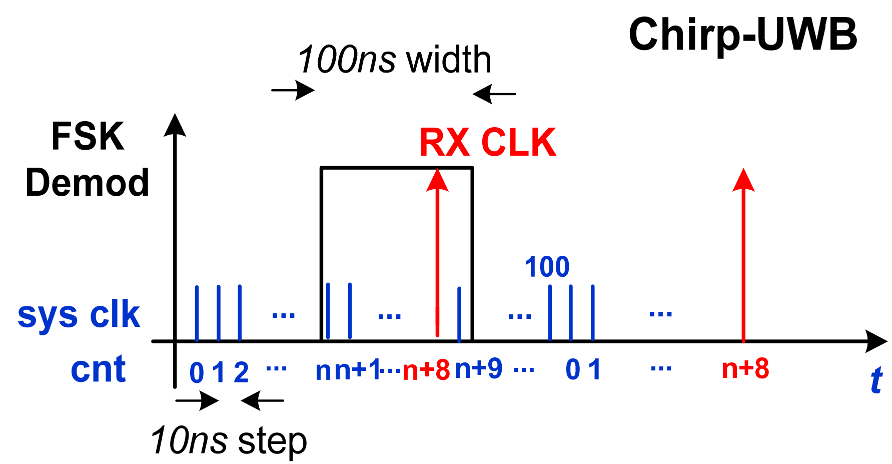
- **Easy and fast bit synch** ☺
- **Moderate peak** power ☺
- **Good spectrum shape** and efficiency ☺
- **Low power** with 10% duty cycle ☺

Bit Synch with Oversampling

Previous designs 1



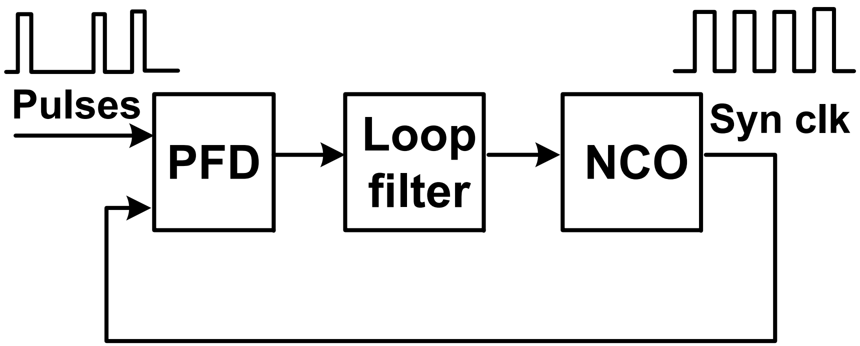
This design



- **Sliding window** in IR-UWB needs complex algorithm with long latency
- **Oversampling** with 100 MHz is simple and fast
- Robust to the clock skew

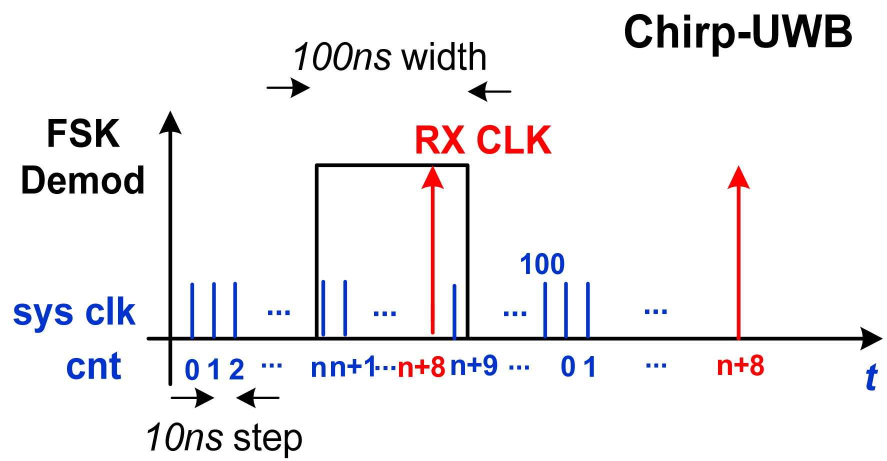
Bit Synch with Oversampling (Cont.)

Previous designs 2



CDR
[ISSCC13, Vigraham]

This design

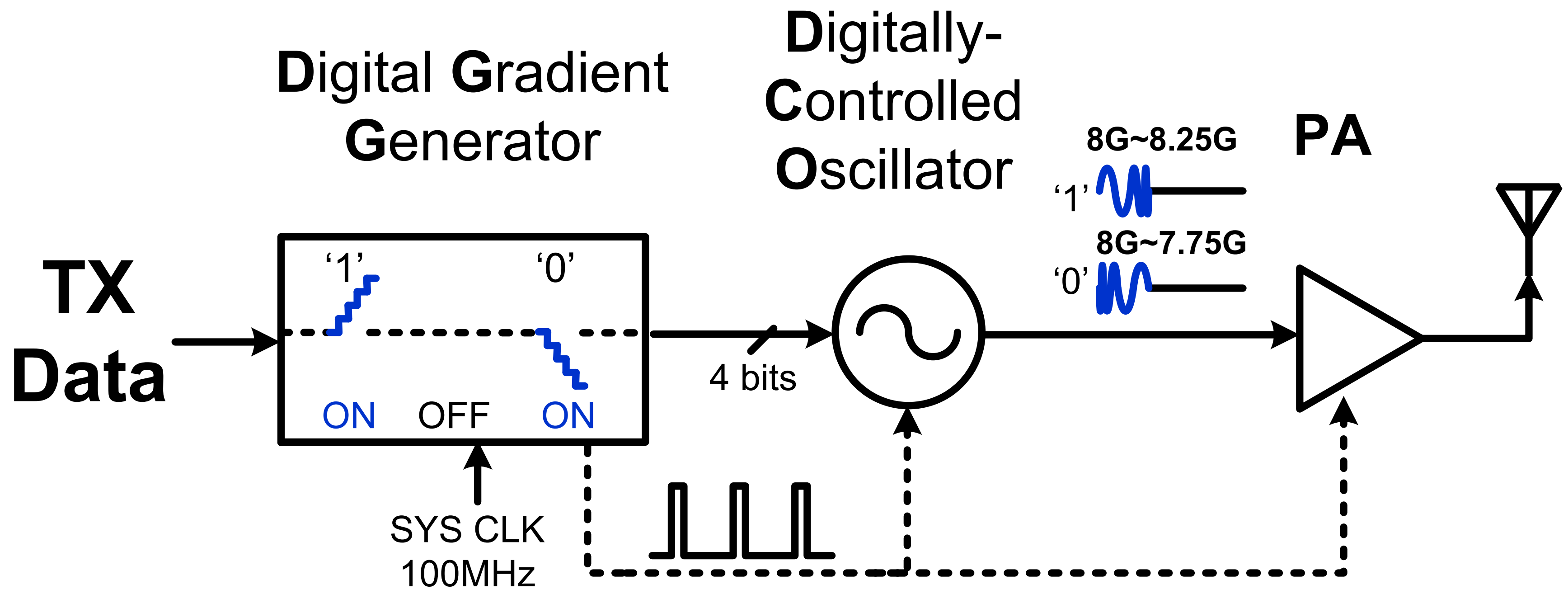


- **CDR** uses a loop for clock recovery with circuit complexity and latency
- **Oversampling** without feedback is fast and simple

Outline

- Background
- Chirp-UWB Technique
- **Transceiver Design**
  - **Digital-intensive UWB generation**
  - **Double-balanced FM demodulation**
- Measurement Results
- Summary

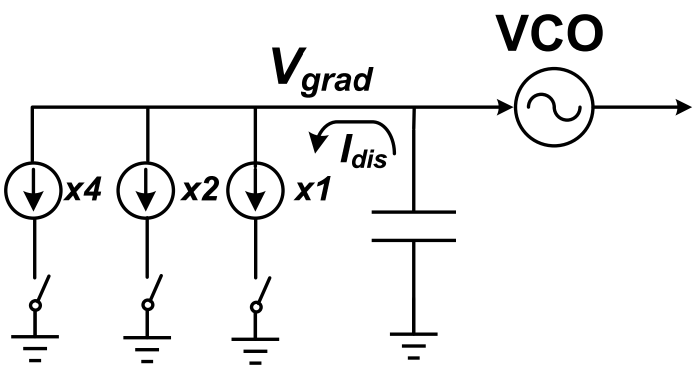
Transmitter Block Diagram



- **Digital intensive**: Open-loop DCO with DGG
- **10% duty-cycling** to save power

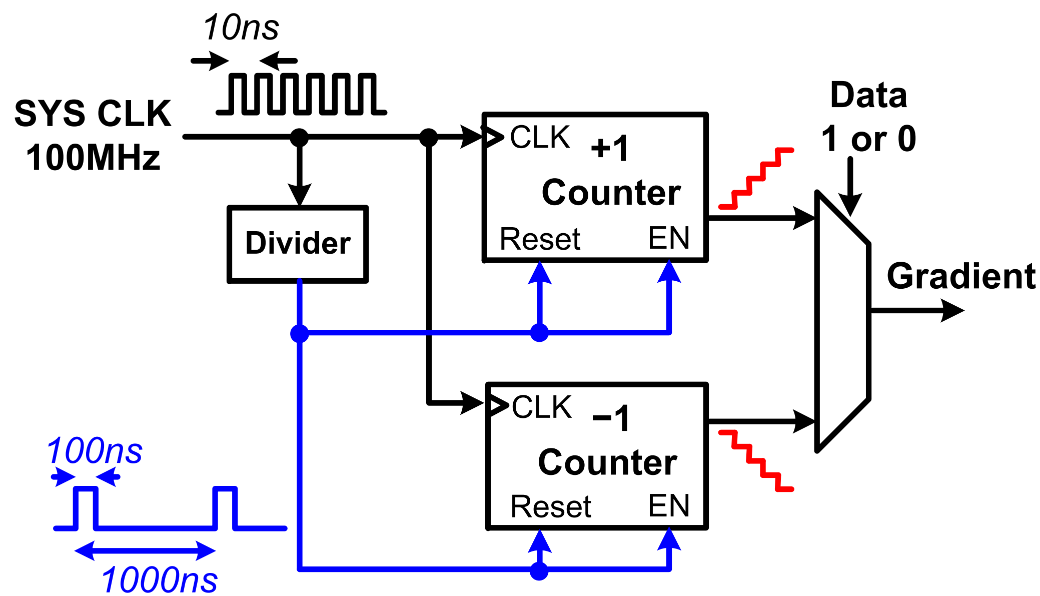
Digital Gradient Generator

Previous designs



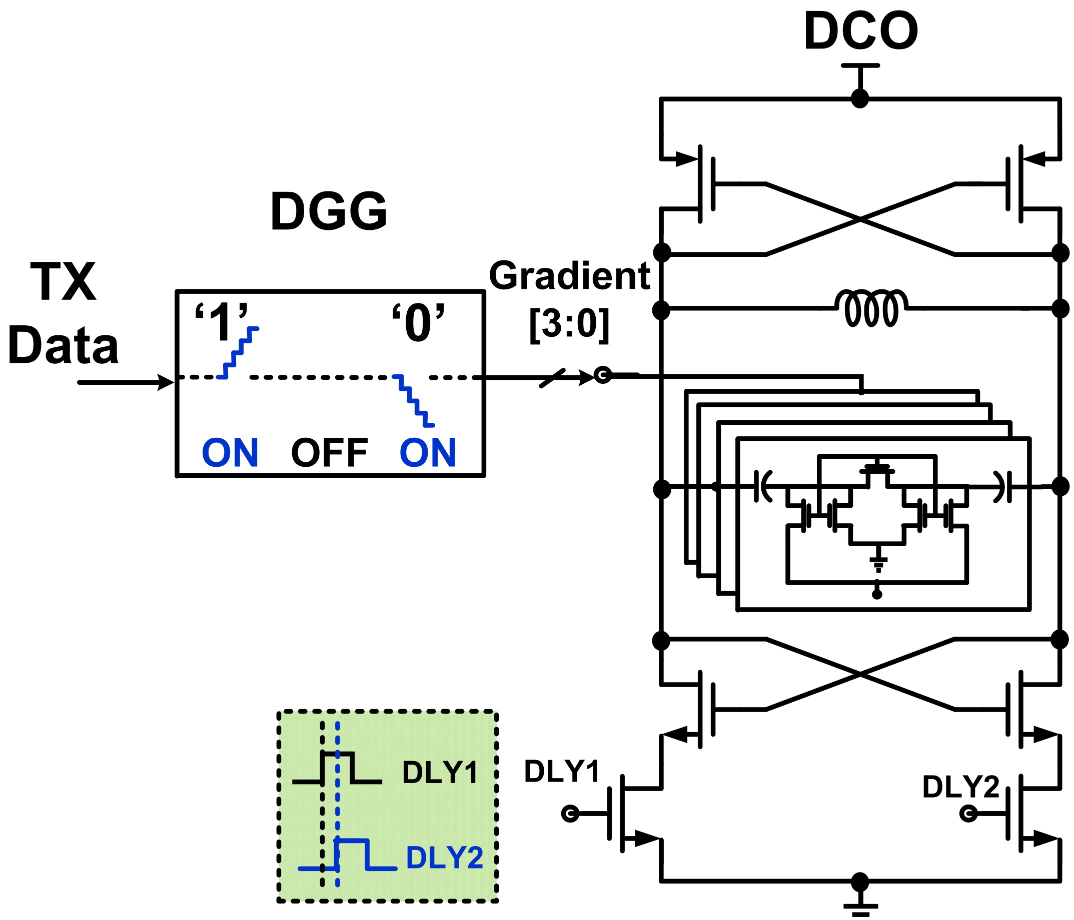
Analog Gradient
[JSSC10, Nair]

This design



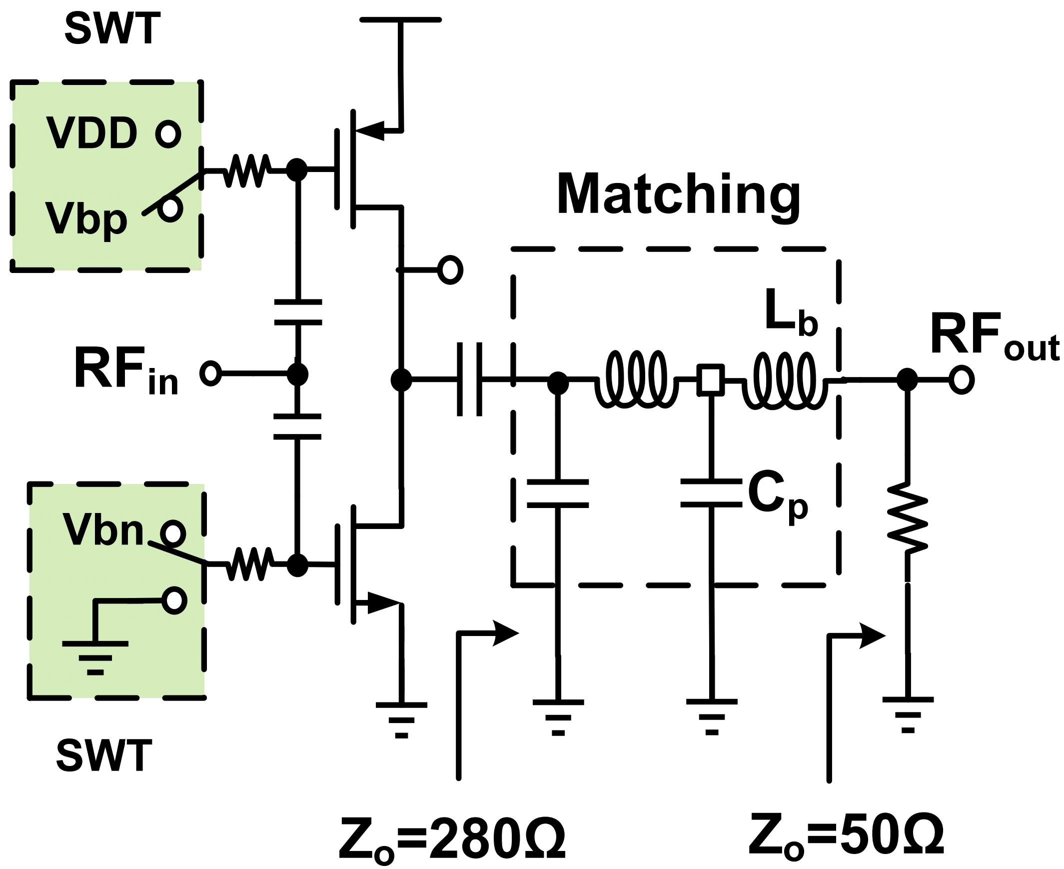
- Digital gradient is **robust to PVT** variations
- **Precise control**: 10-ns time resol. 4-bit amp resol.
- **Small** chip area

Digitally-Controlled Oscillator



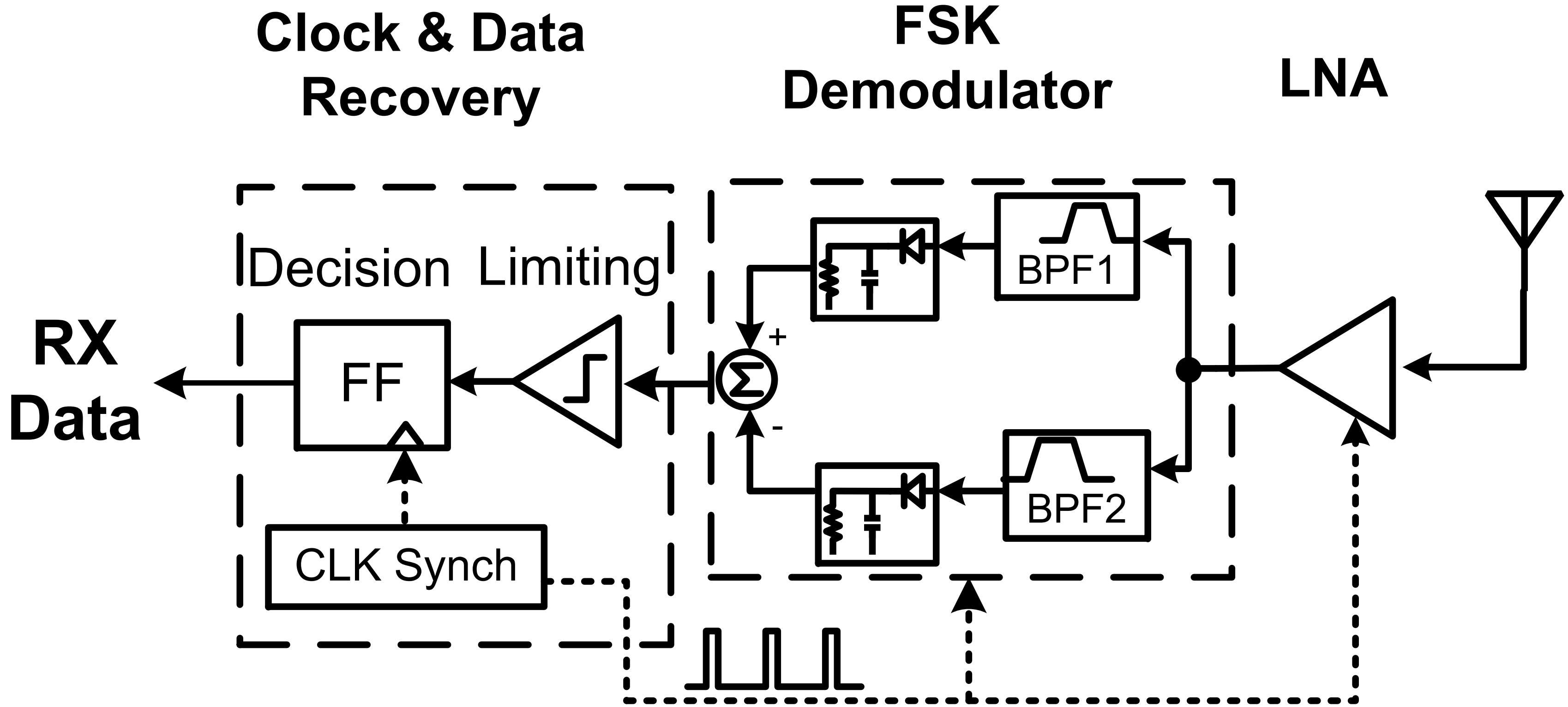
- **Fast start-up** DCO for 100ns chirps
  - Gating and fast start-up by the tail control
- 25 MHz/LSB

Class-AB Power Amplifier



- 2-section output matching and load pull
- **Gating** at the bias voltage

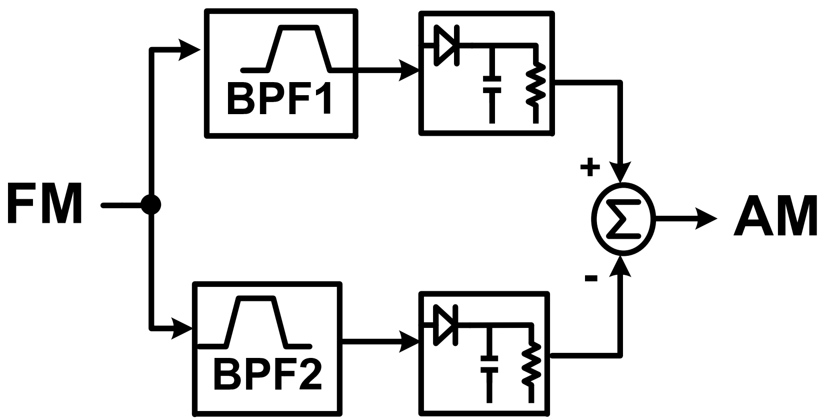
Receiver Block Diagram

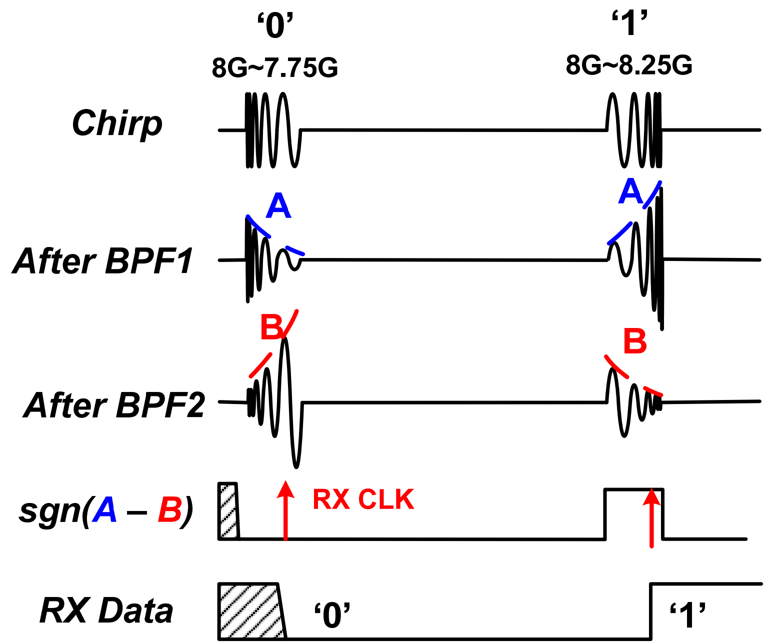


- Non-coherent **Double-balanced** FM demodulator
- **Oversampling** CDR
- **15% gating** to save power

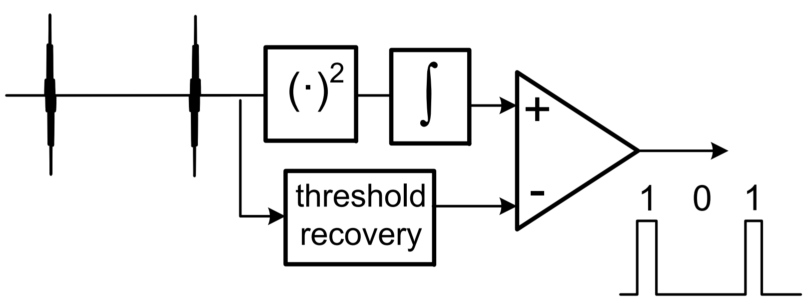
Frequency Detection

Frequency detection





Energy detection

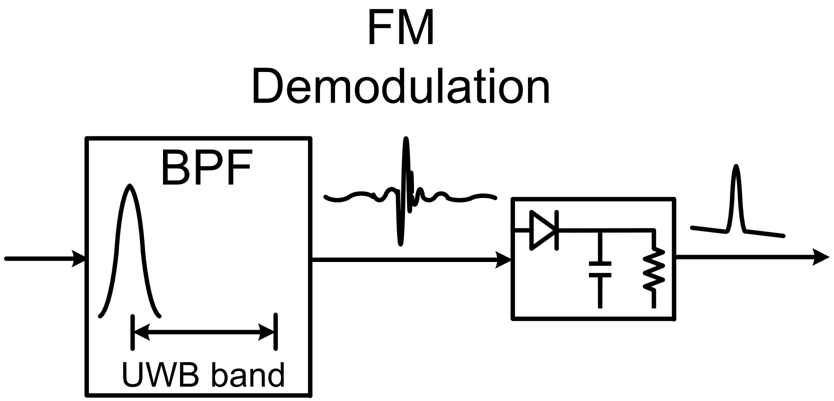


[ISSCC13, Vigraham]

	Threshold Generation	Noise Impact
Frequency detection	No Need	Small
Energy detection	Needed	Big

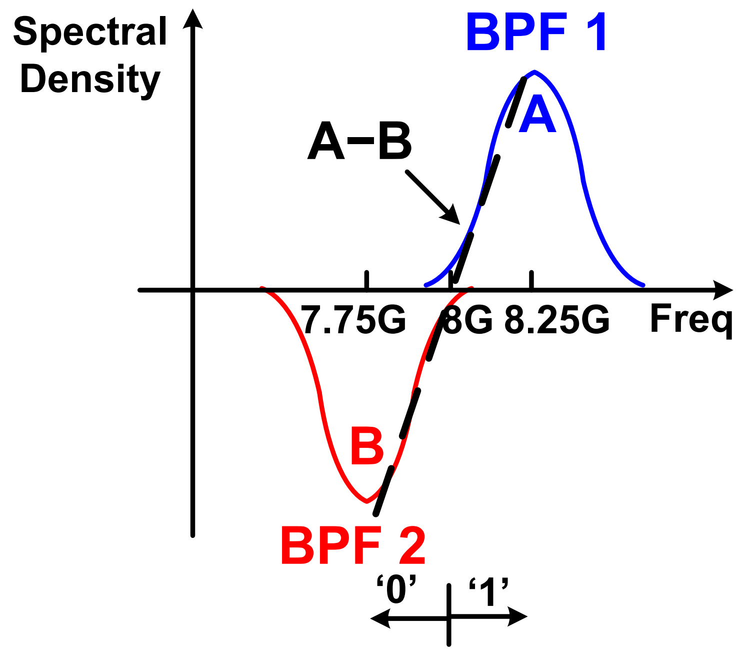
Wideband BPFs

Previous designs



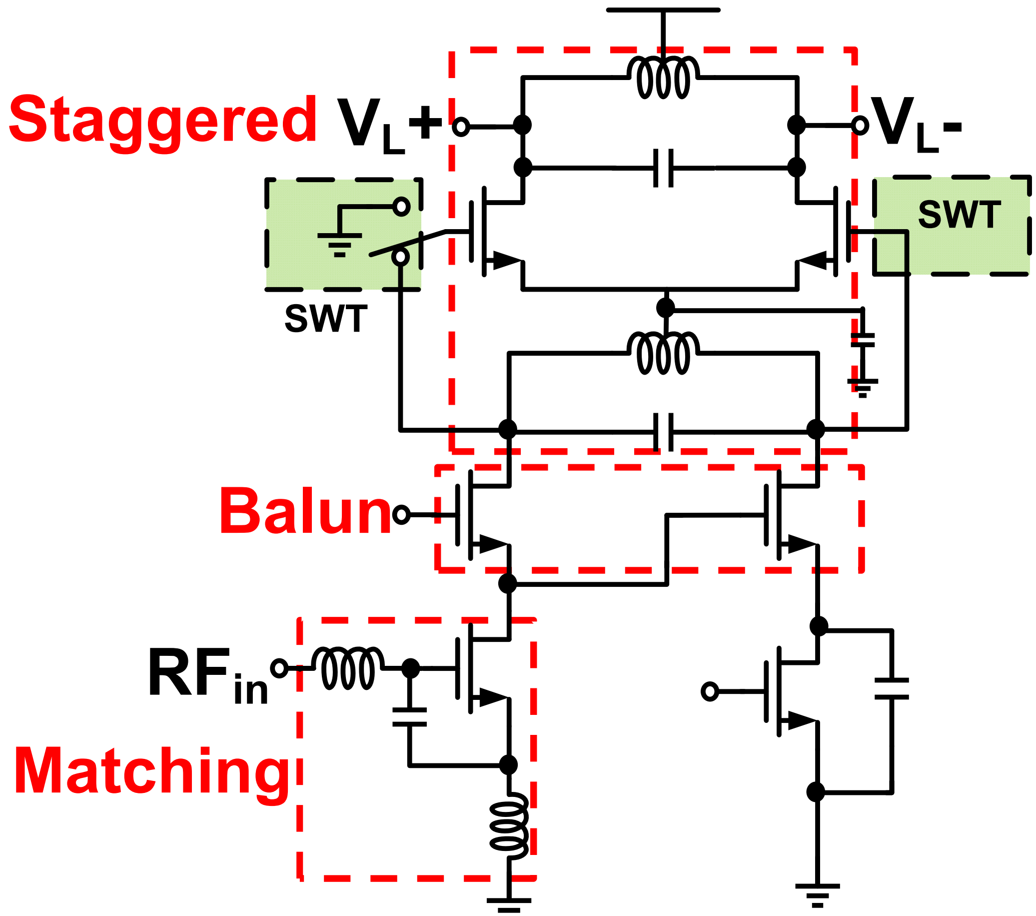
NB BPF
[MTT 2011, Saputra]

This design



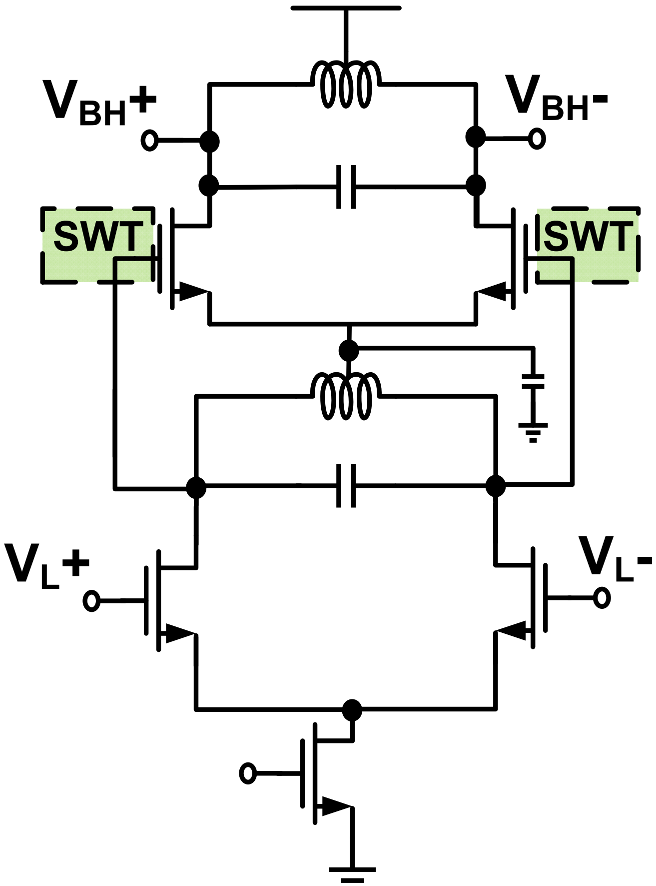
- Wideband BPFs cover whole UWB sub-band
- **High linearity** to ease the demodulation
- Relax **inductor-Q requirement** for CMOS integration

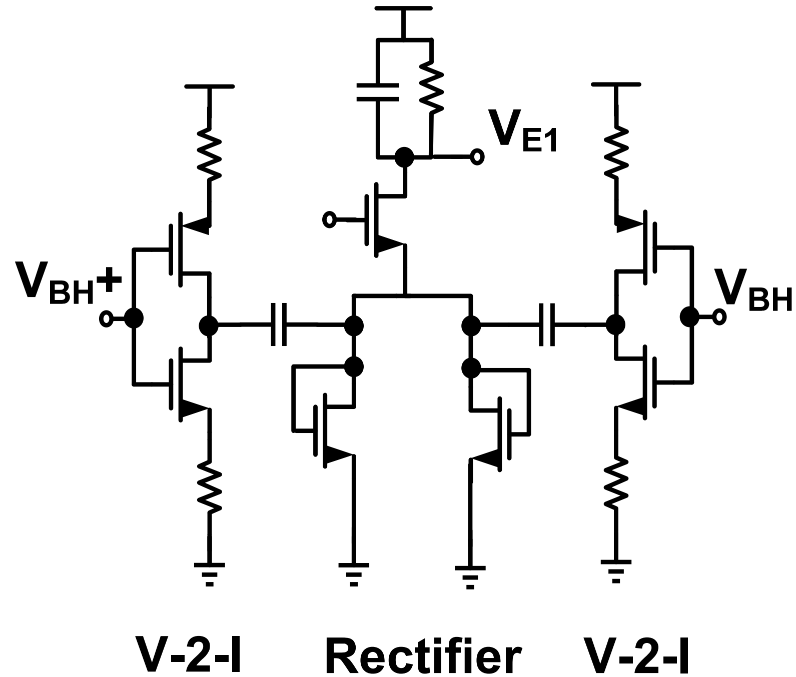
Wideband LNA



- Three-stage stacked to **reuse current**
- **Gating** at the top transistors

BPFs and Envelope Detectors





- 4^{th} Butterworth BPFs with **gating on top stage**
- Envelope detectors with full-wave current rectifier

Outline

- Background
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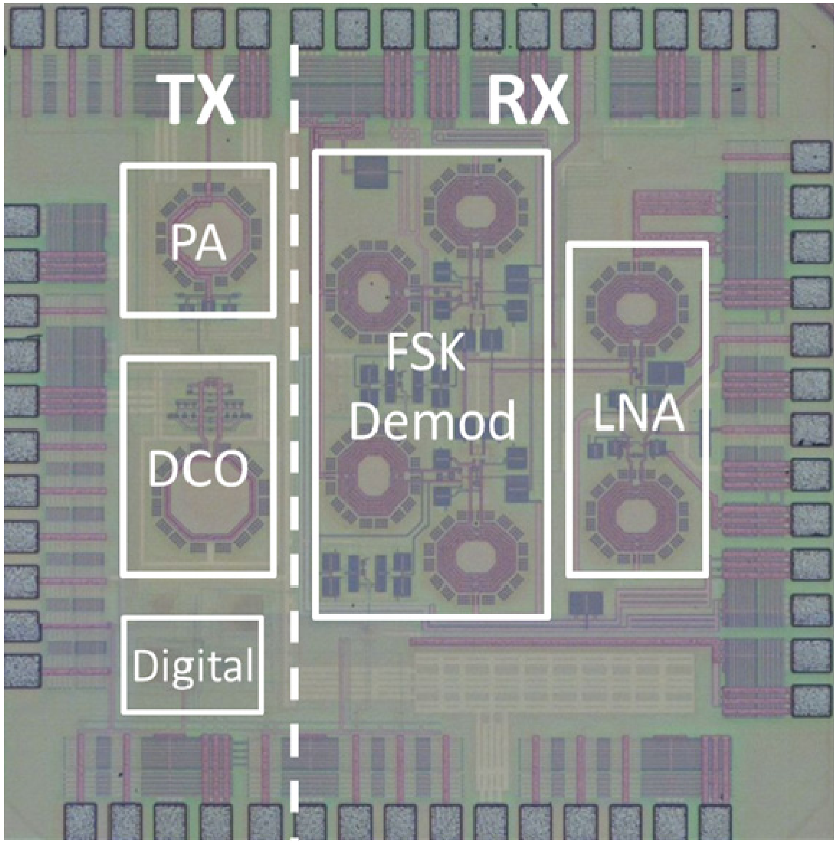
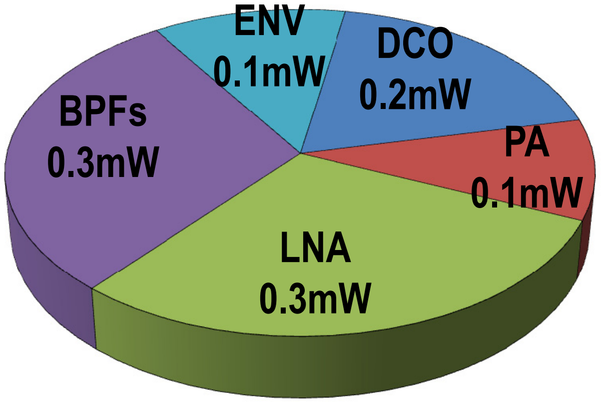
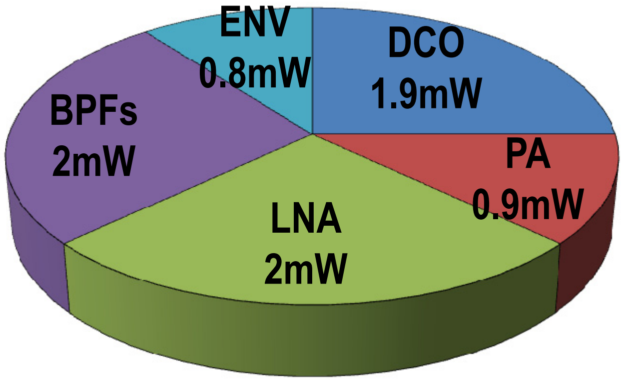
Prototype and Power Consumption



Average power (total: 1mW)

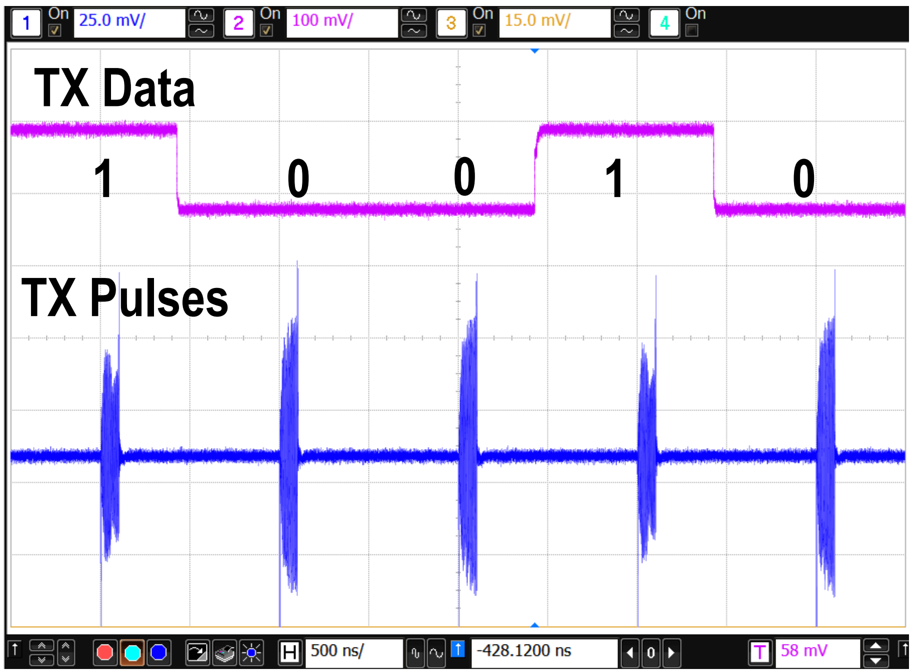


Peak power (total: 7.6mW)

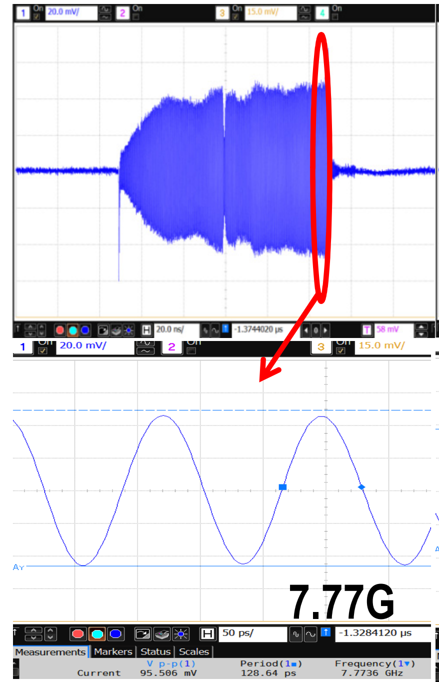


- CMOS 65nm, 1.5mm x 1.5mm

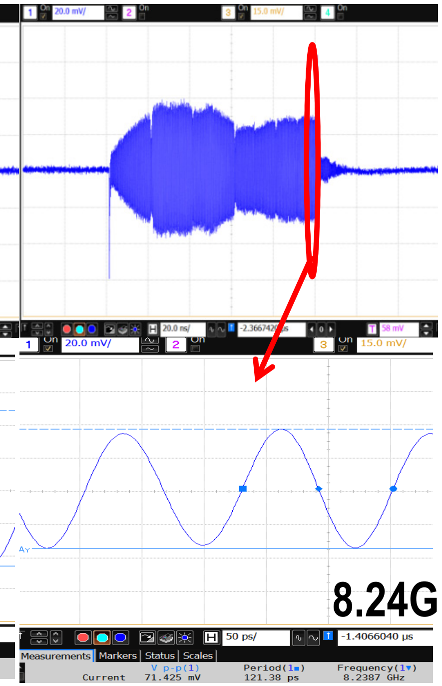
Transmitter Pulse Waveforms



Chirp '0'
8G->7.75G



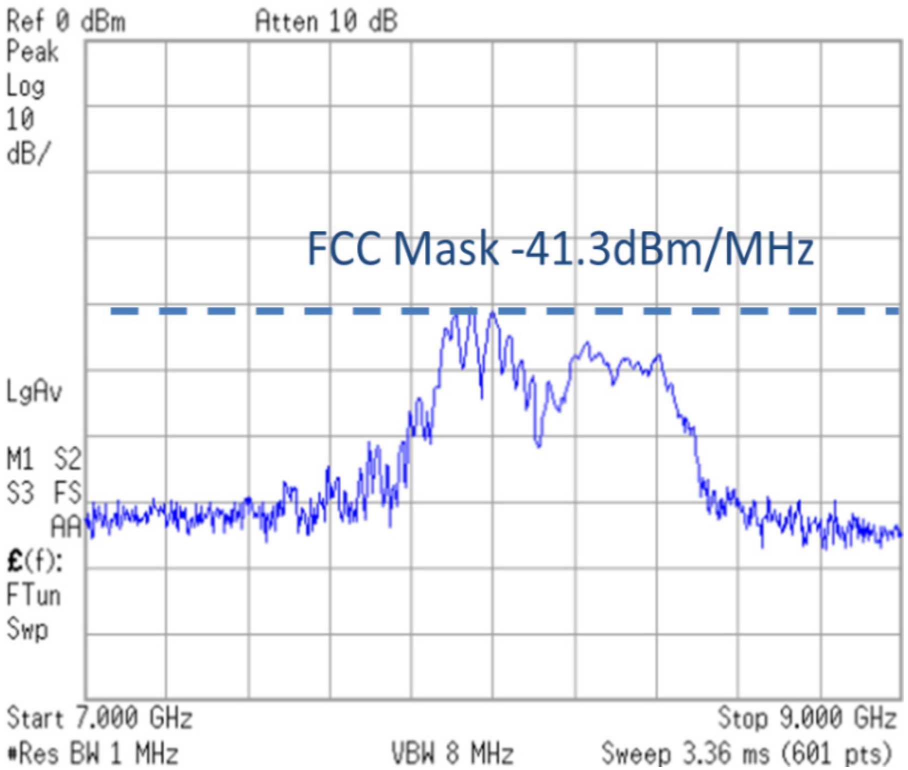
Chirp '1'
8G->8.25G



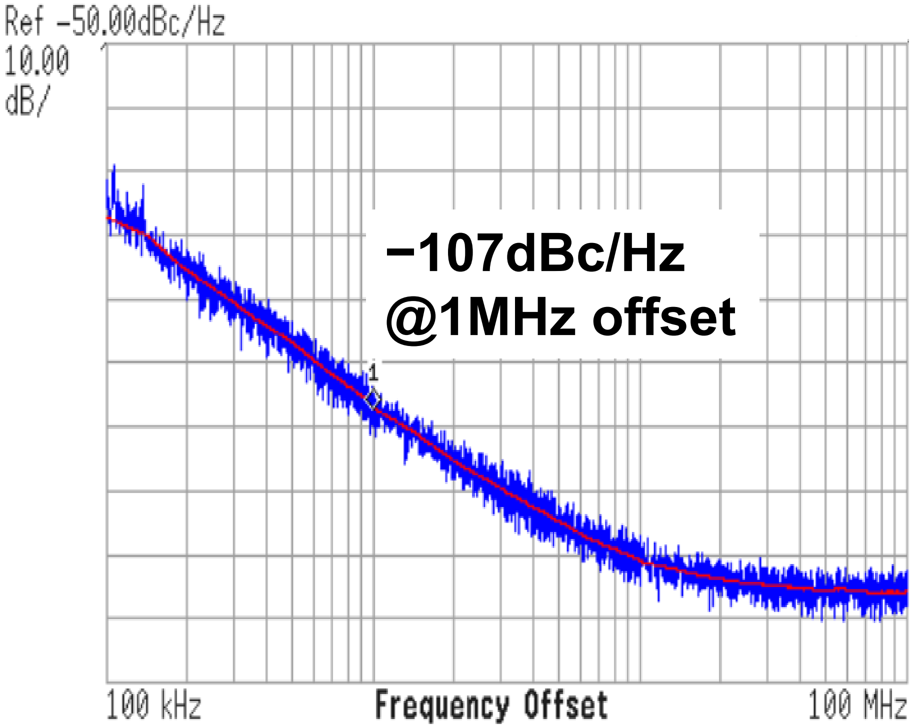
- Chirp pulses with 10% duty cycle
- Frequency descending/ascending as expected

Transmitter Power Spectrum

TX Spectrum

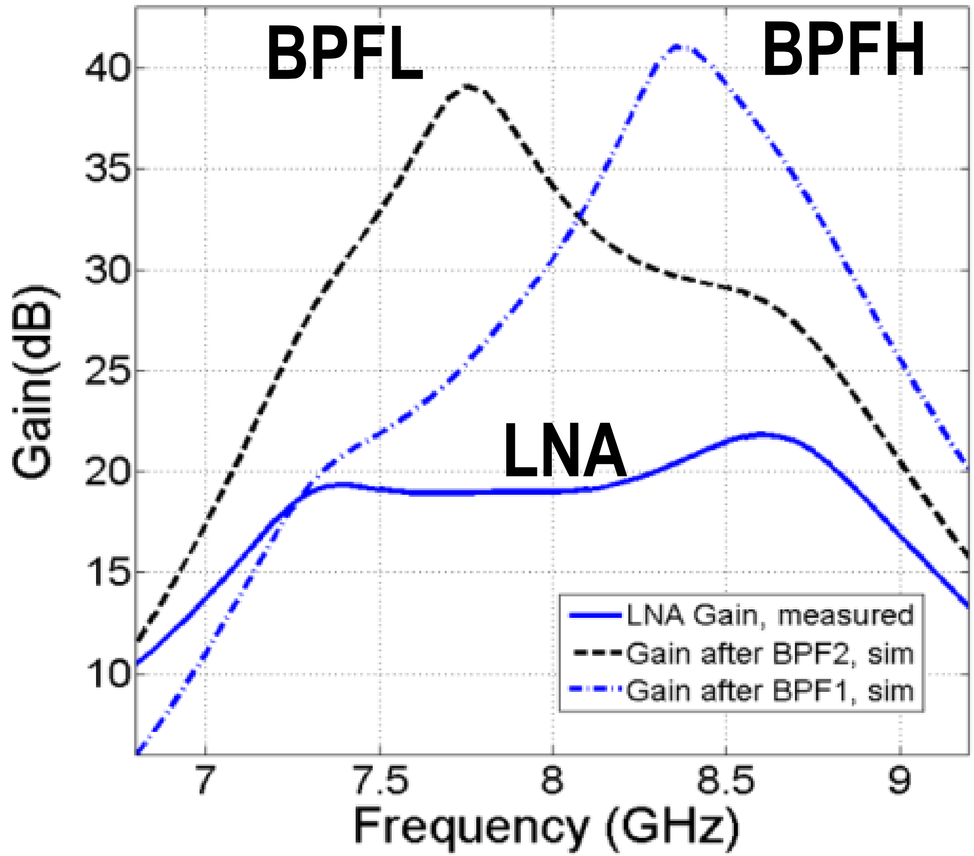


DCO Phase Noise



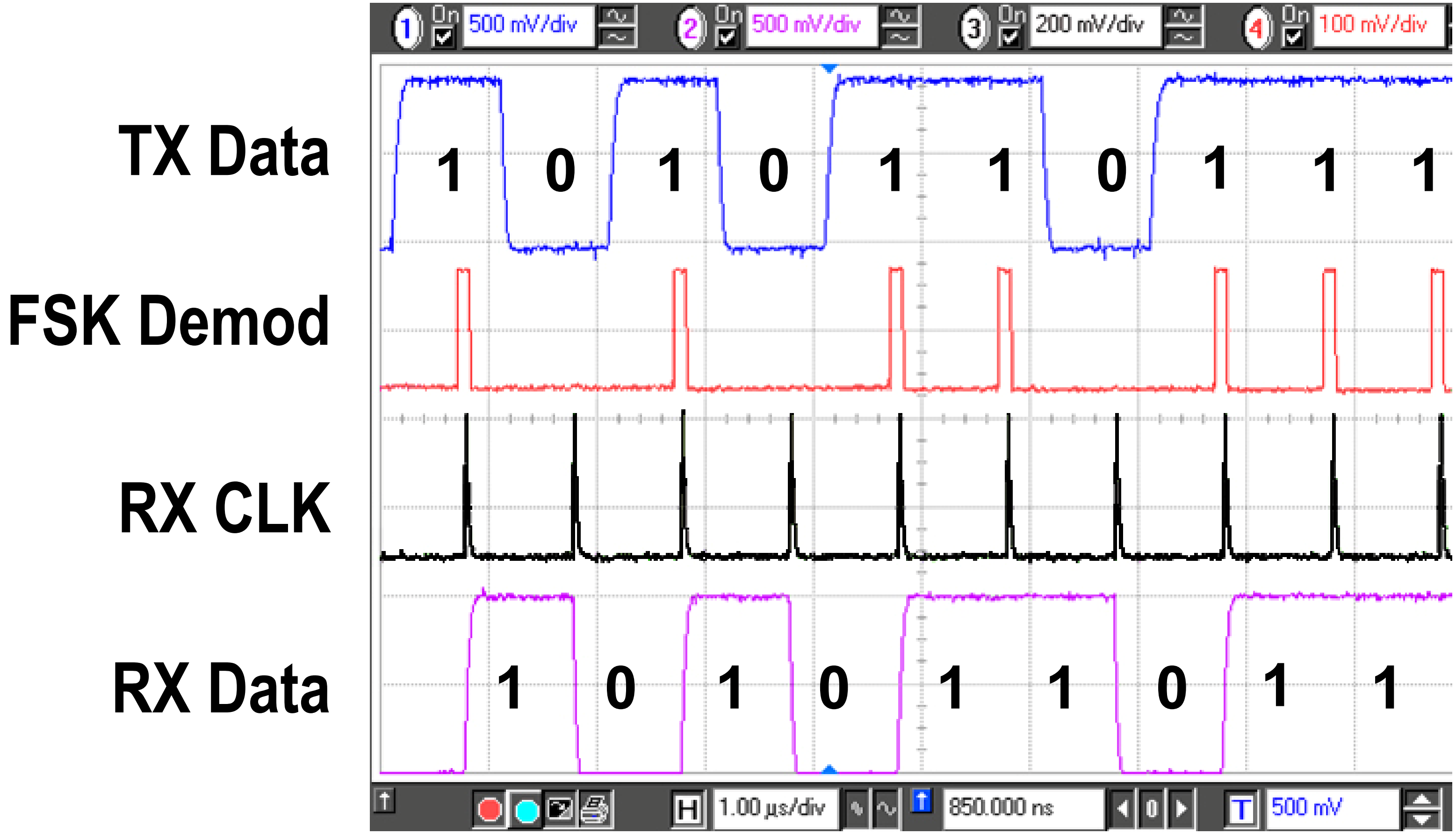
- Fulfills FCC spectrum mask
- Free-running DCO provides sufficient phase noise

Receiver's Frontend Gain



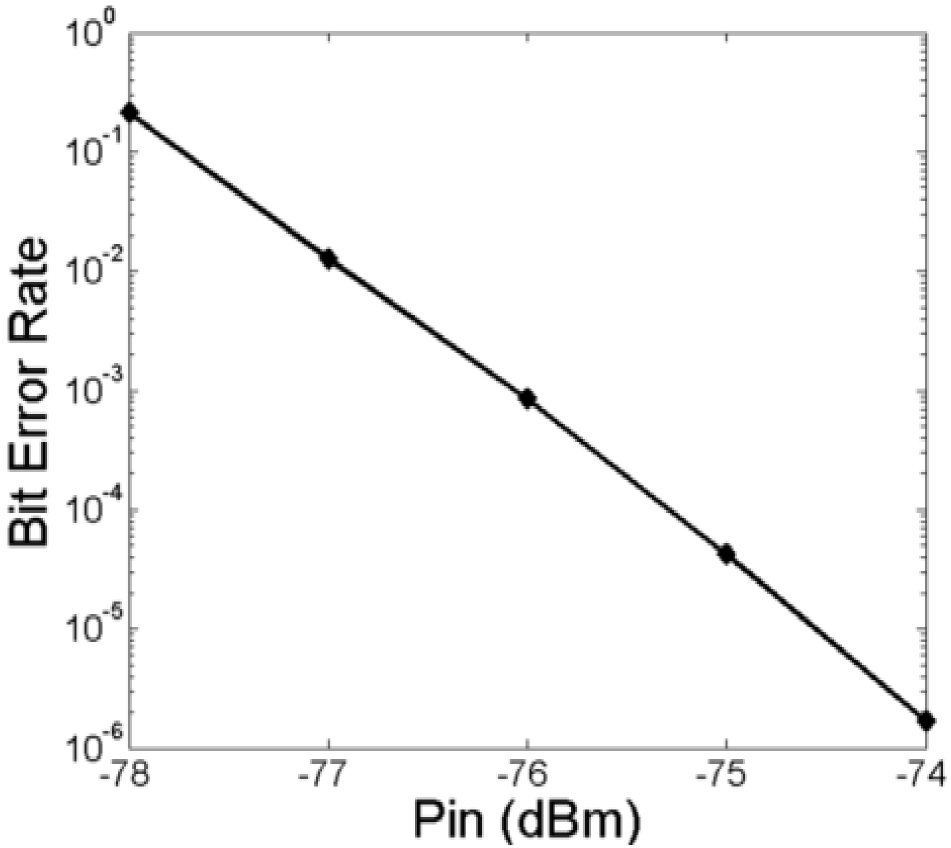
- Broadband LNA gain covers whole band
- Two BPFs provides > 10dB amp difference for demod

Clock and Data Recovery



- CLK is recovered by 100MHz oversampling
- The CLK samples the demod to recover Data

Bit Error Rate

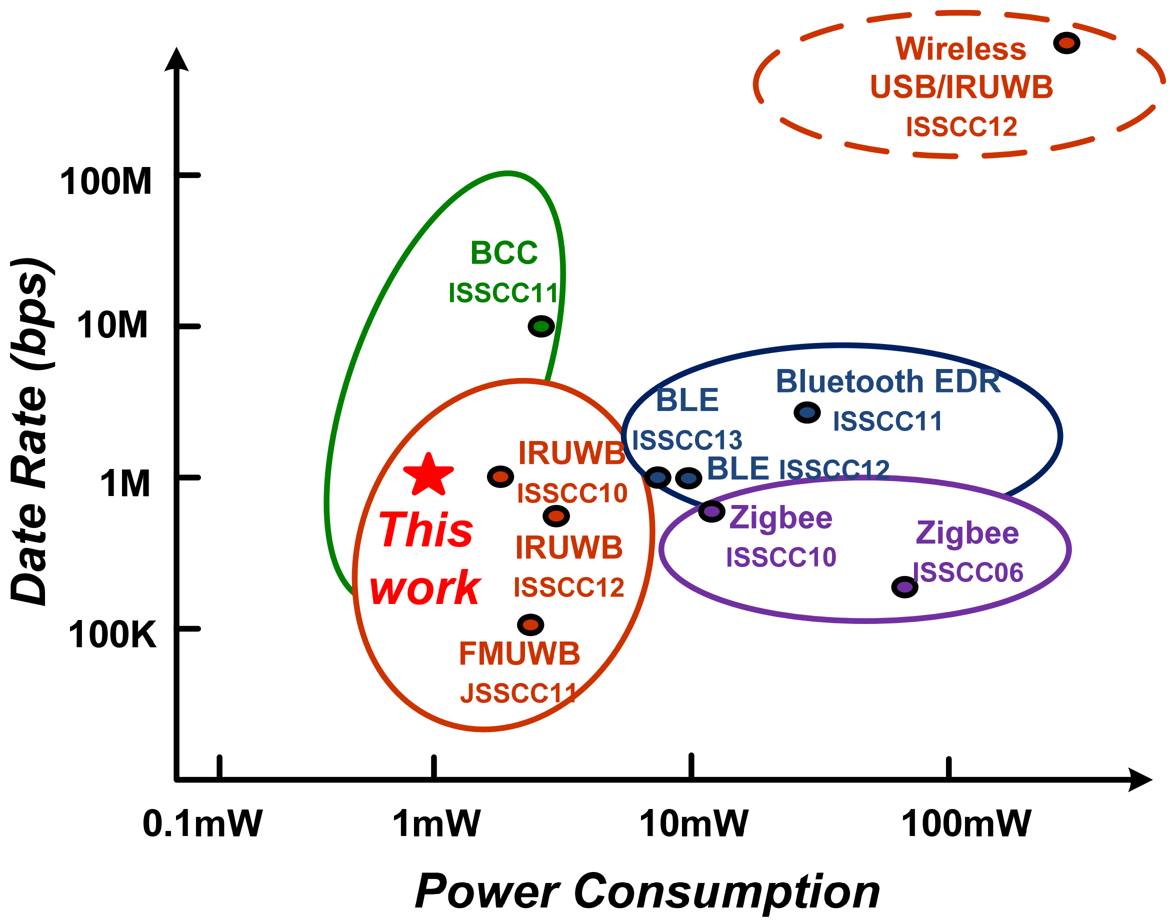


- Receiver's sensitivity is –76 dBm
- To be further improved by adding frontend gain

TRX Performance Comparison

	ISSCC2012 Wang	JSSC2011 TMTT2011 Saputra	ISSCC2013 Liu	ISSCC2012 Wong	JSSC2010 Nair	This work
PHY	IR-UWB	FM-UWB	Bluetooth LE	Bluetooth LE	Chirp-UWB	Chirp-UWB
Frequency	6-9GHz	3.75-4.25GHz	2.4GHz	2.4GHz	3.15-3.9GHz	7.75-8.25GHz
Data rate	0.85Mb/s	0.1Mb/s	1Mb/s	1Mb/s	4Mb/s	1Mb/s
Power (P_{TRX})	6.5mW	3.1mW	9.2mW	9.4mW	56.8mW	1mW
Energy/bit	7.6nJ/bit	31nJ/bit	9.2nJ/bit	9.4nJ/bit	14.2nJ/bit	1nJ/bit
Sensitivity	-88dBm	-84dBm	-98dBm	-94dBm	-84dBm	-76dBm
Tech.	90nm	90nm/65nm	90nm	130nm	180nm	65nm
Active Area	2mm^2	0.77mm^2	2mm^2	5.9mm^2	6.7mm^2	0.7mm^2

Comparison to Other TRXs



Outline

- Background
- Chirp-UWB Technique
- Transceiver Design
  - Digital-intensive UWB generation
  - Double-balanced FM demodulation
- Measurement Results
- **Summary**

Summary

- 1mW 1Mb/s transceiver in 65nm CMOS.
- Chirp-UWB technique:
  - Reduced peak transmitter power (< IR-UWB)
  - Relaxed bit synch complexity (< IR-UWB)
  - Lower power with duty cycle (< FM-UWB)
- Sub-mW Mb/s transceiver is feasible with chirp-UWB and enhanced duty-cycled operation.

Thanks for your attention !

A 0.5V 1.15mW 0.2mm^2 Sub-GHz ZigBee Receiver Supporting 433/860/915/960MHz ISM Bands with Zero External Components

Zhicheng Lin[1], Pui-In Mak[1,2] and Rui P. Martins[1,2,3]

1 – State-Key Laboratory of Analog and Mixed-Signal VLSI

University of Macau, Macao SAR, China

2 – UMTEC, Macao, China

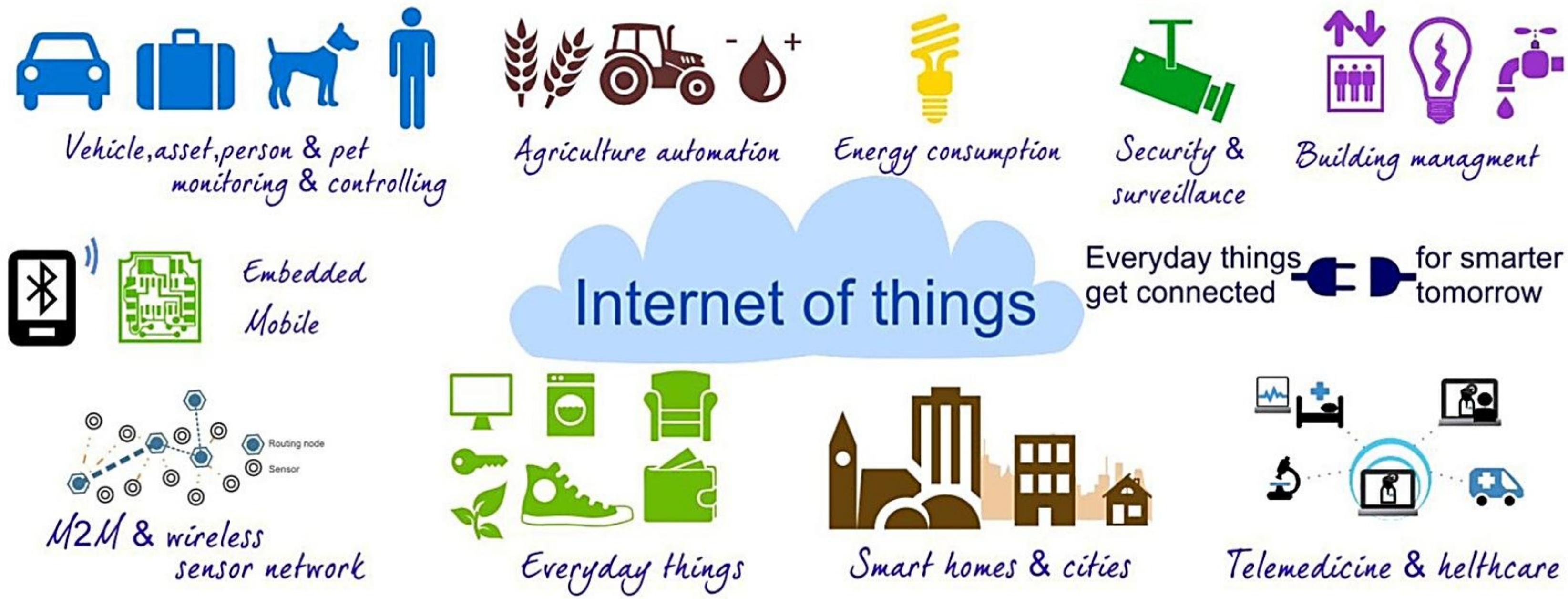
3 – Instituto Superior Técnico, U of Lisbon, Portugal

ISSCC 2014

Outline

- Introduction
- Brief review of prior art
- Proposed Function-Reuse Receiver (RX)
- Experimental results
- Comparison and conclusion

Introduction



http://www.cio.co.ke/news/main-stories/

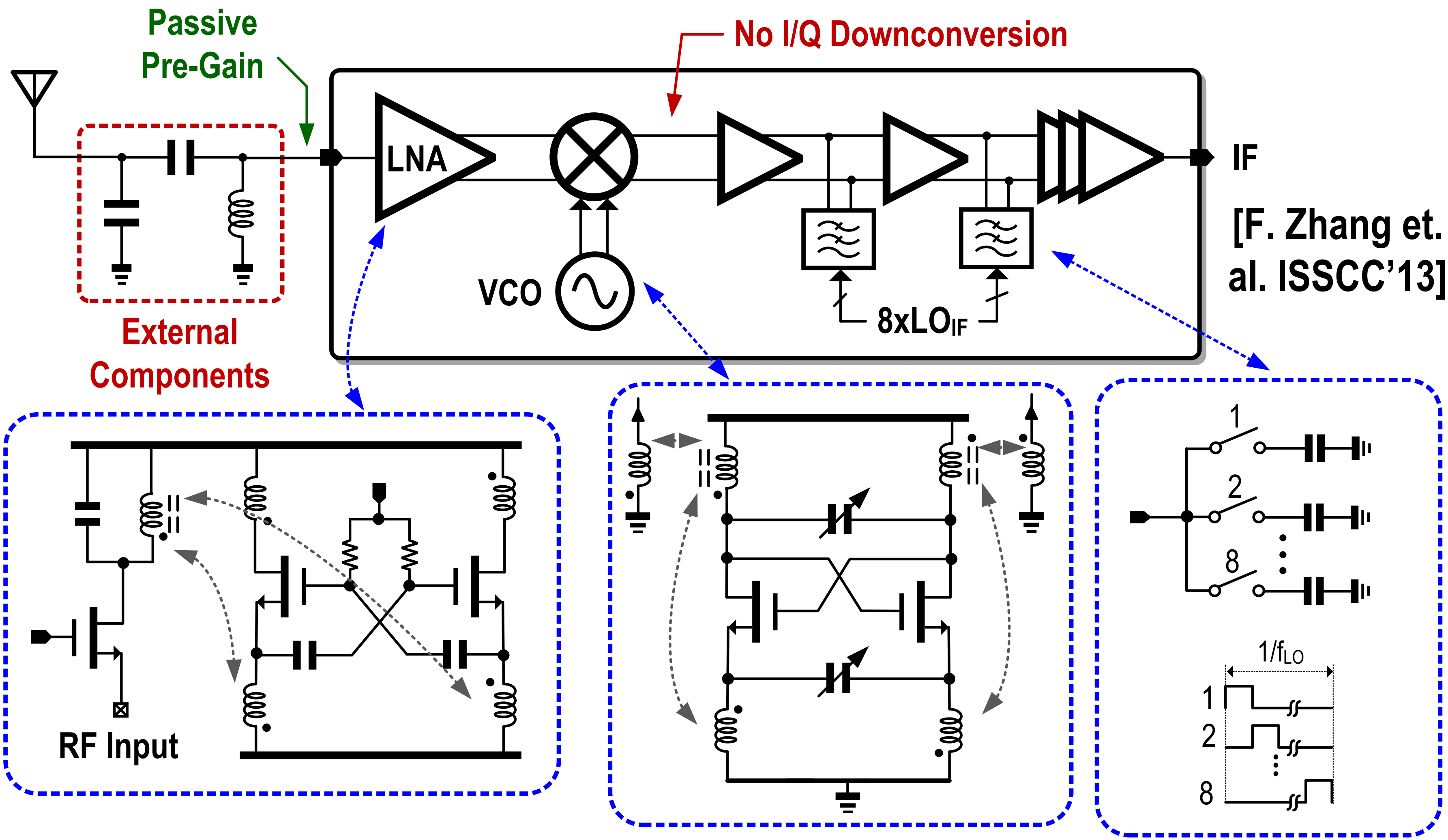
Sub-GHz ISM bands in different regions:

☑ 430 - 434 MHz : China ☑ 868 - 869 MHz : Europe

☑ 902 - 928 MHz : America ☑ 950 - 956 MHz : Japan

A multi-ISM-band ZigBee receiver with small power, area and zero external components

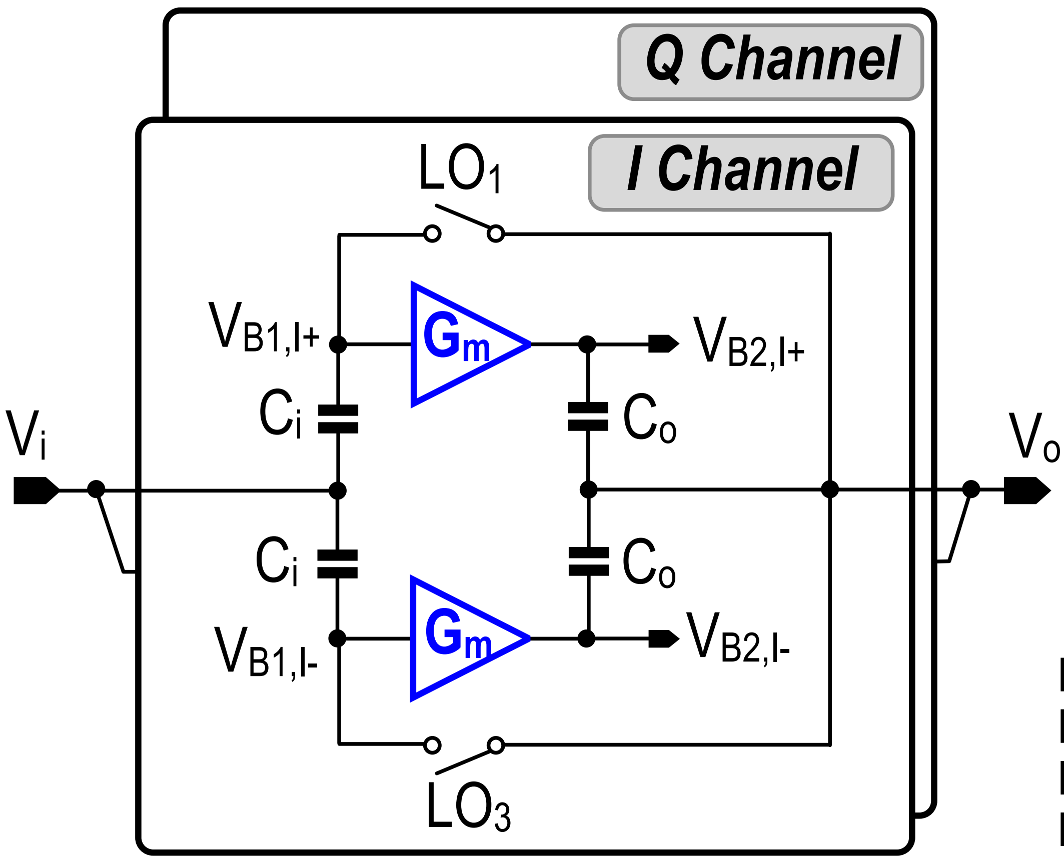
Prior Art: Ultra-Low-Voltage Receiver

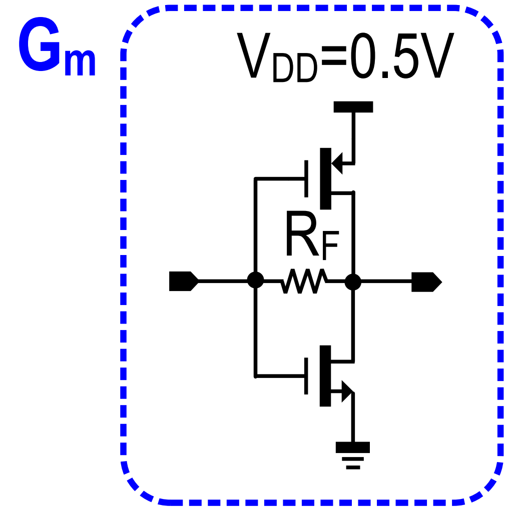


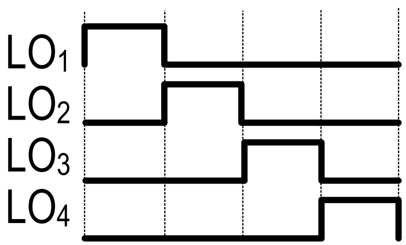
☑ Low voltage (0.3V) and low power (1.6mW)

☒ Large area (2.5mm^2) and single band only (2.4GHz)

Proposed RF-to-BB Function-Reuse RX



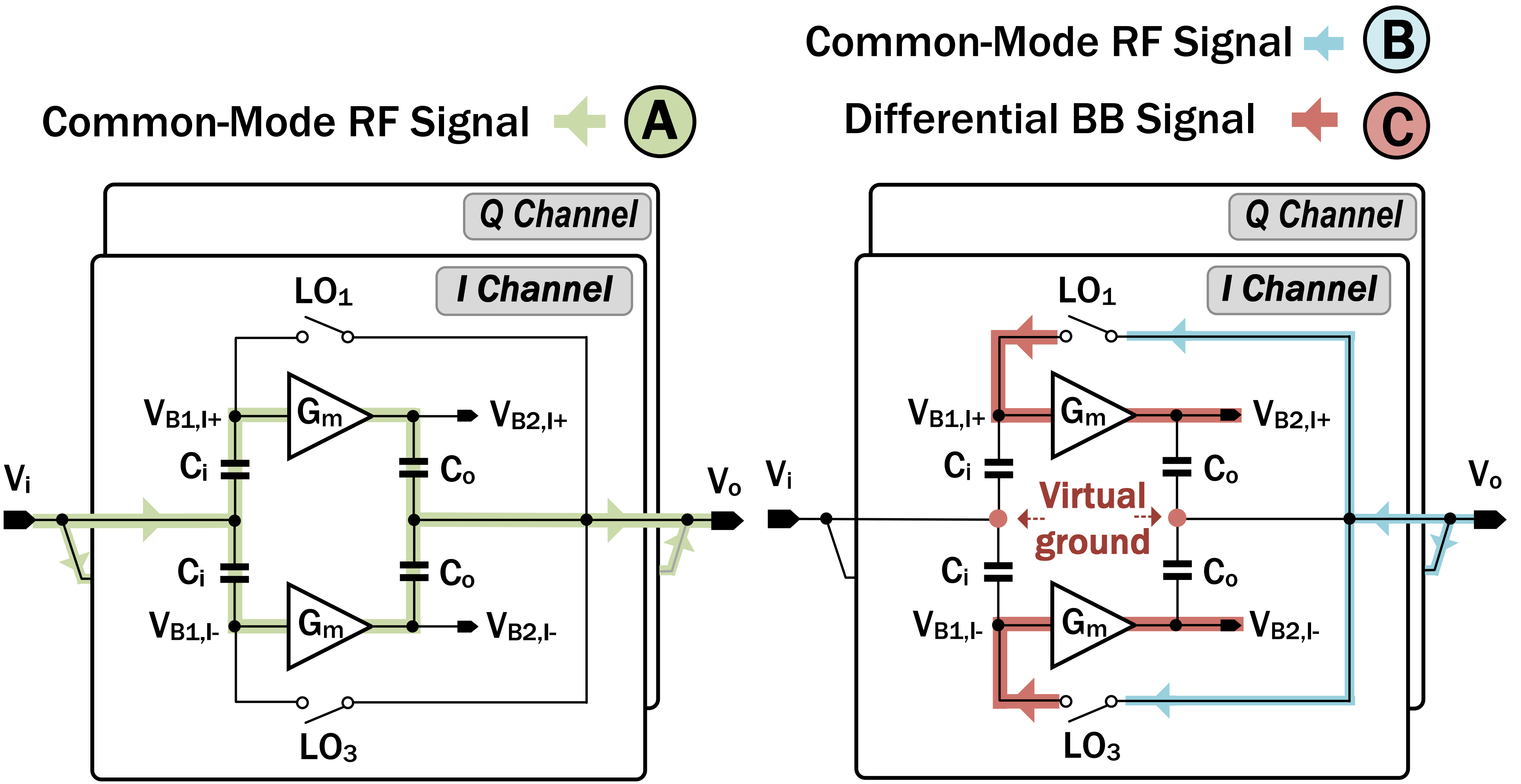




4-Phase
25% LO

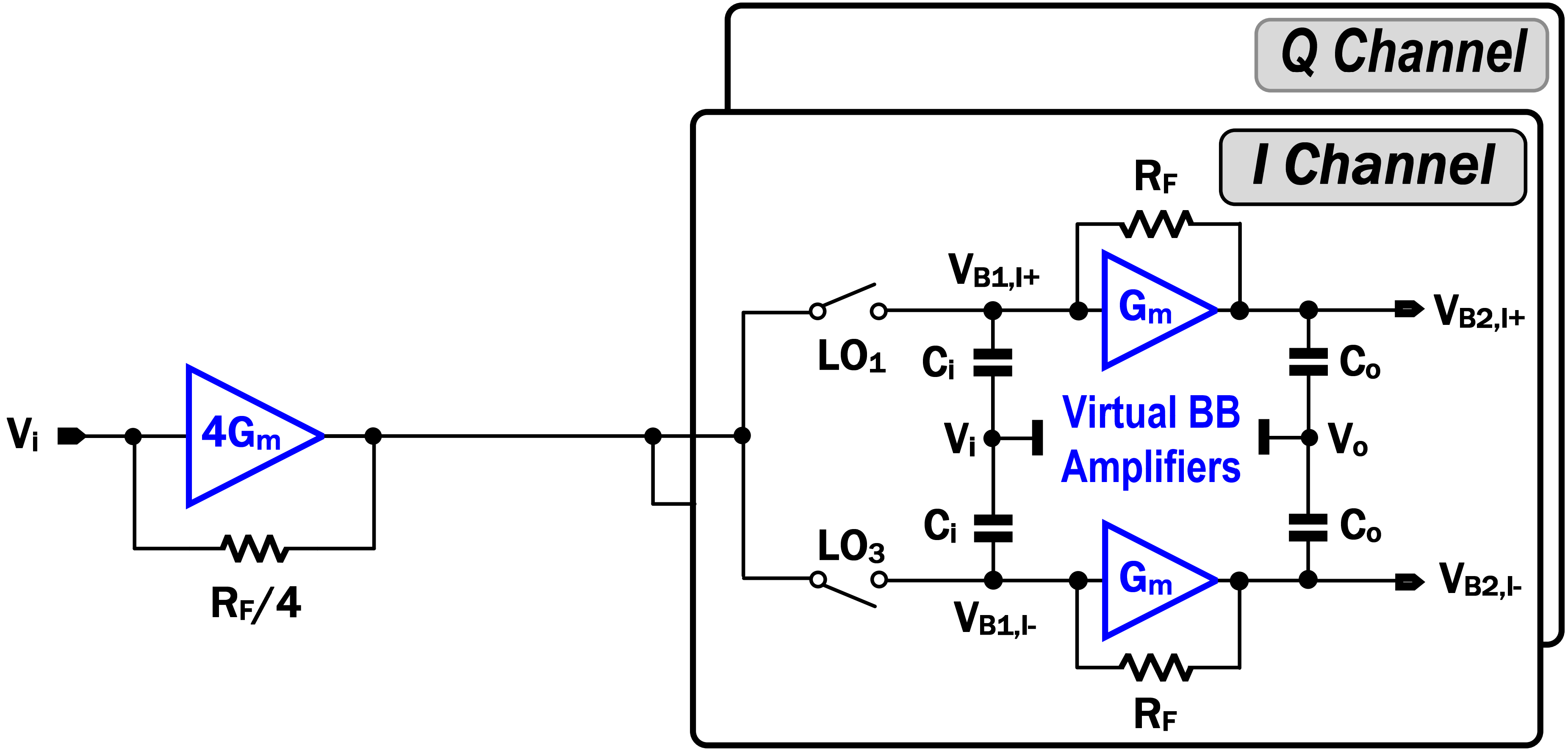
- ☑ Low-voltage and function reuse ➔ **good power efficiency**
- ☑ No external components and on-chip inductors ➔ **low cost**
- ☑ LO-defined center frequency ➔ **multi-band operation**

Operating Principle of the RX



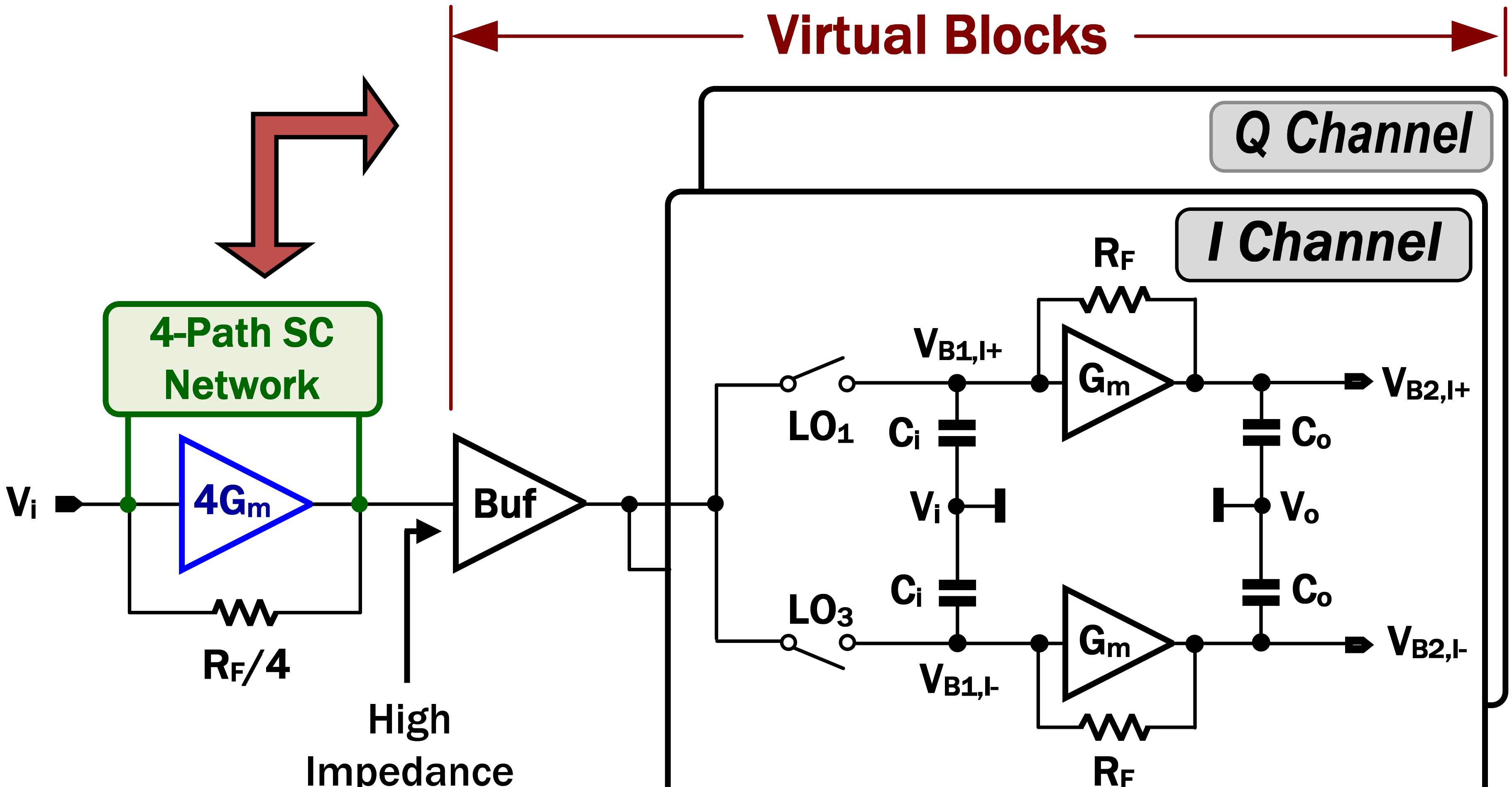
☑ **Virtual BB amplifiers shared with the RF amplifier**

Functional View of the RX - 1



☑ $4G_m$ at RF for low NF ☑ $1G_m$ at BB for high IIP3

Functional View of the RX - 2

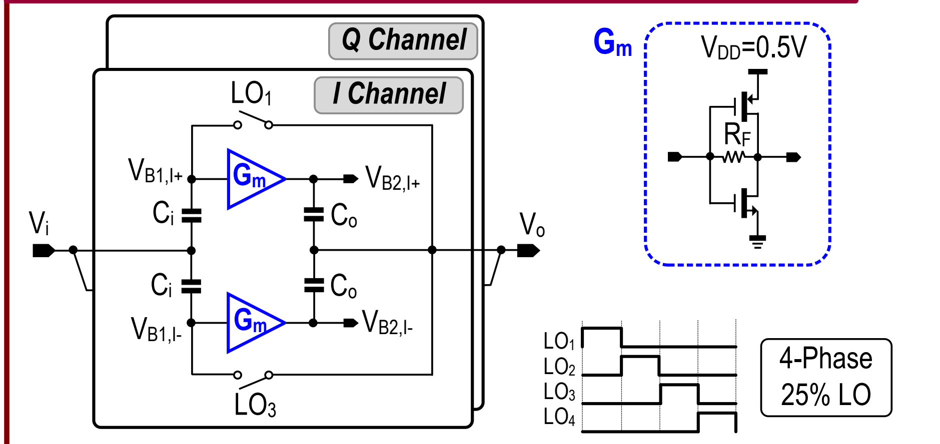


☑ 4-Path SC Network for RF filtering (details later)

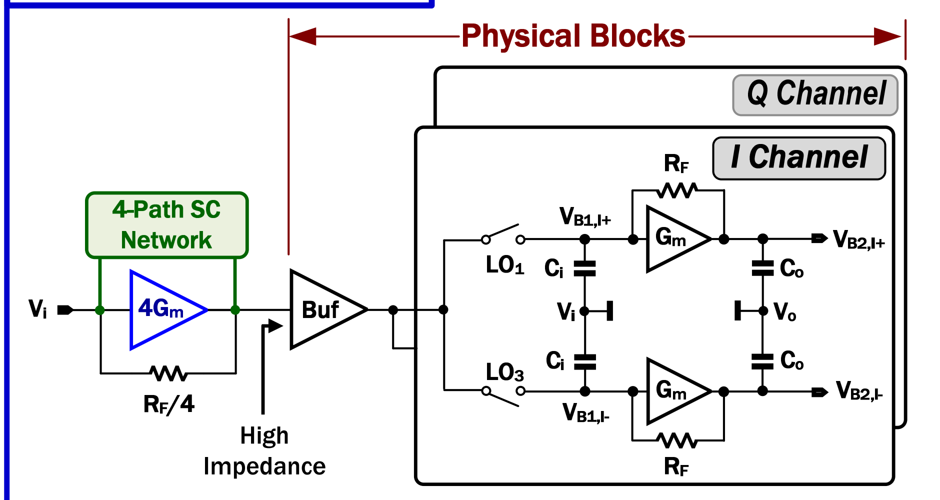
☑ Virtual blocks (reduce power, area and noise)

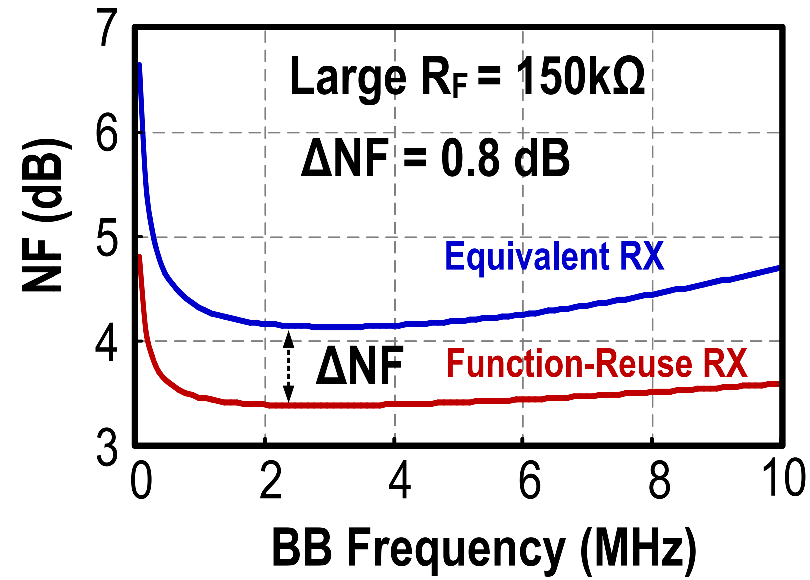
Simulation Results: BB NF

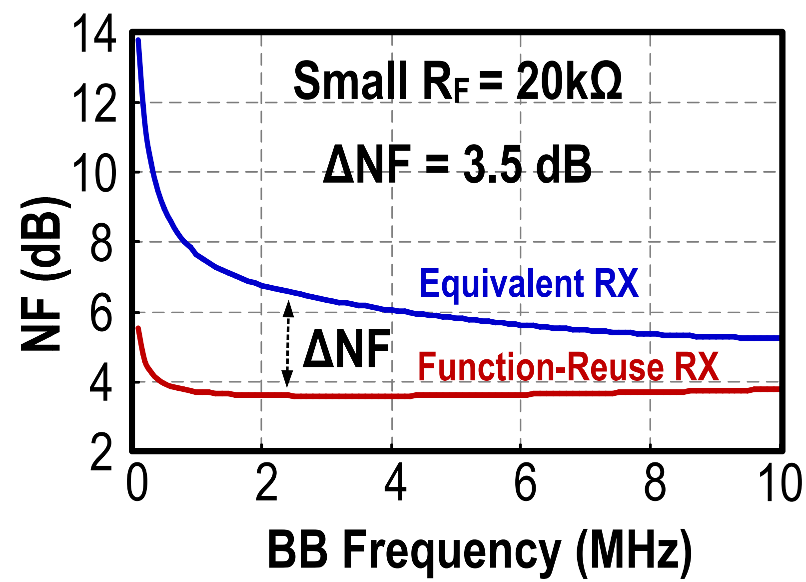
Proposed Function-Reuse RX



Equivalent RX

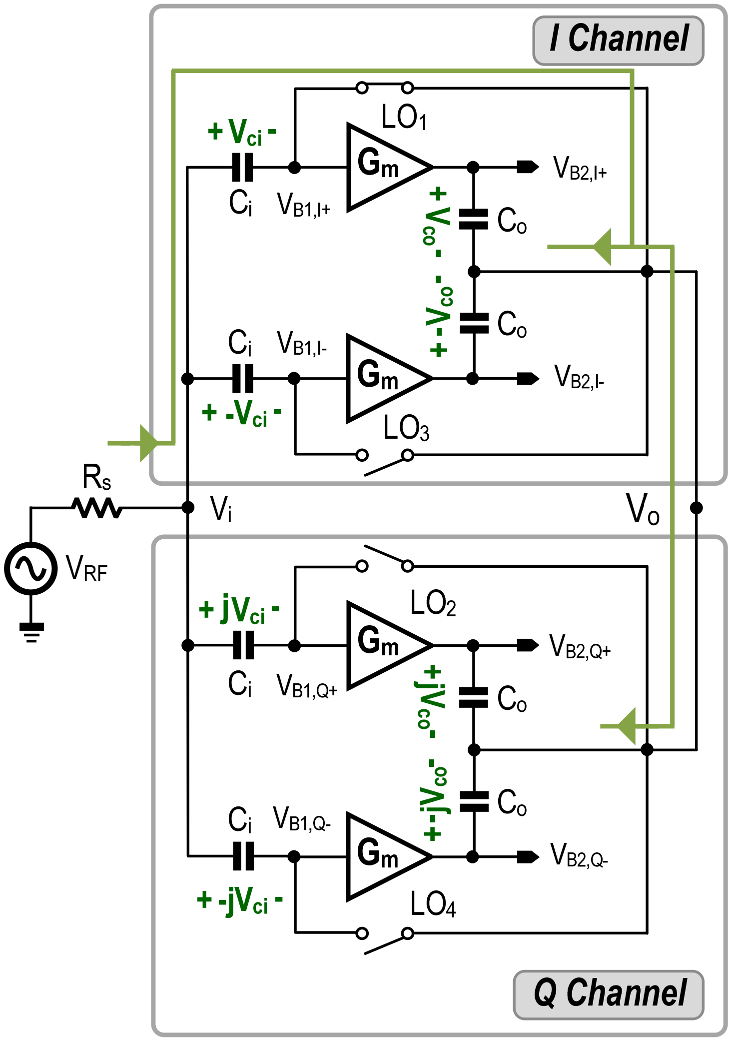


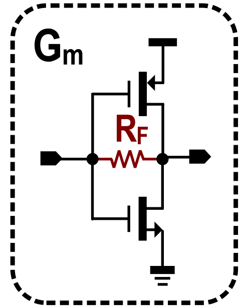


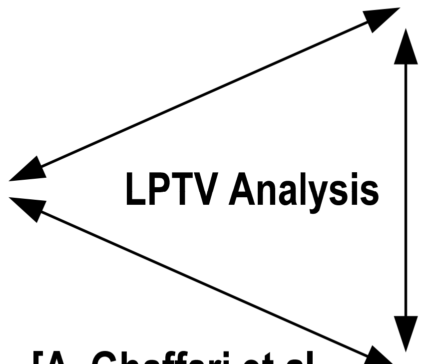


The Family of GB-SC Architecture

This Work

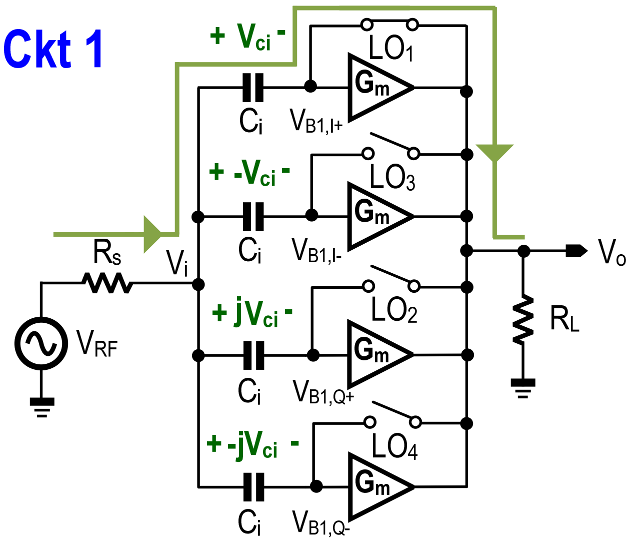




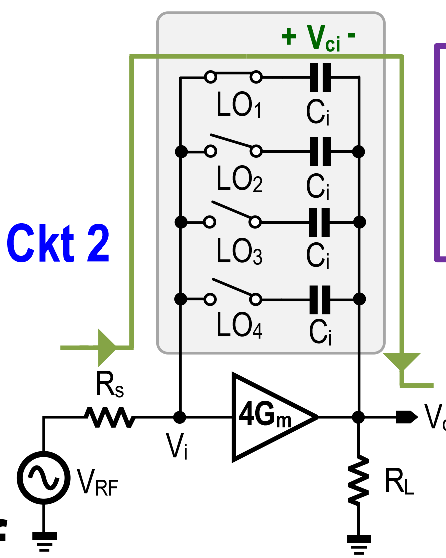


[A. Ghaffari et al., JSSC May'11]

Eq. Ckt 1



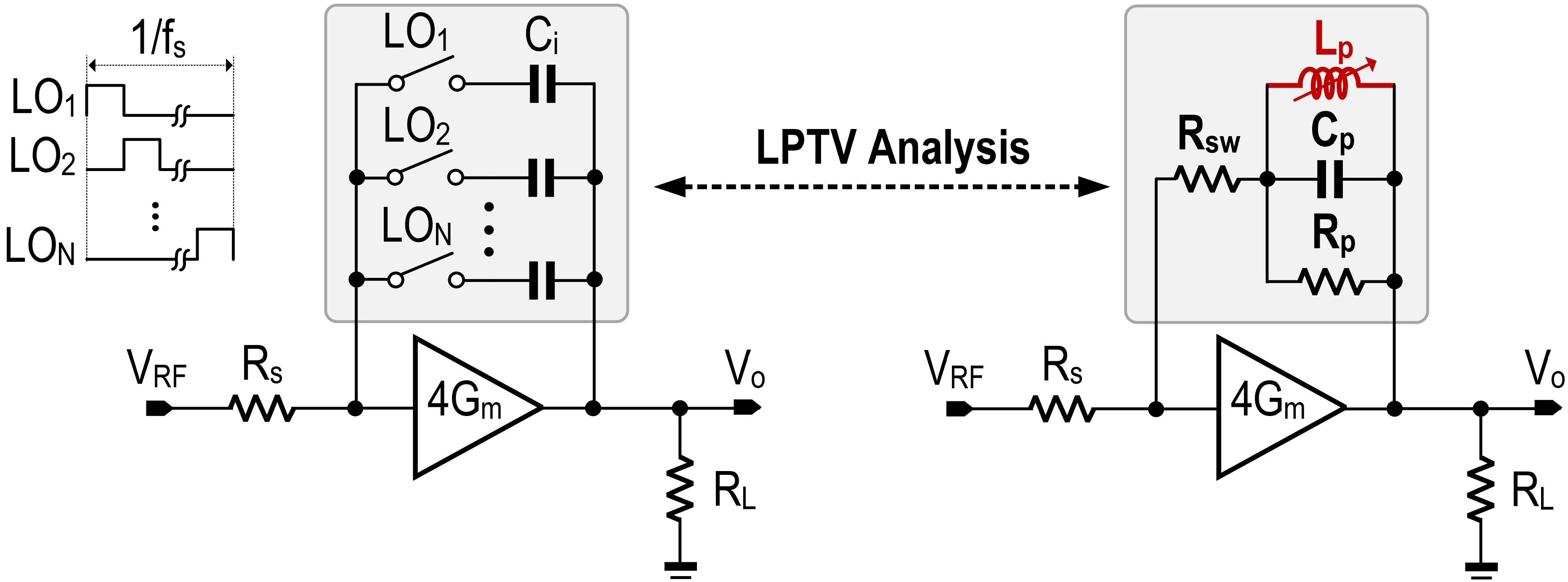
Eq. Ckt 2



Easy for analysis next

If $R_F = \infty$, the three circuits are equivalent @ f_s

N-Path LNA with GB-SC Network



RLC network with a tunable L_p by f_s

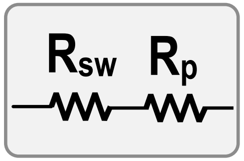
☑ L_pC_p resonant @ f_s ☑ Tunable S_{11} & S_{21} by f_s

☑ Constant RF BW and ultimate OB rejection

Characteristics of the N-Path LNA

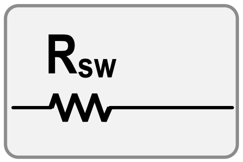
Frequency Selectivity Feedback

@ f_s



(High IB gain)

@ $f_{RF} >> f_s$ or $f_{RF} << f_s$



(Low OB gain)

$$R_{in} \approx \frac{(R_F/4)//R_P}{4G_mR_L} \text{ @ resonant}$$

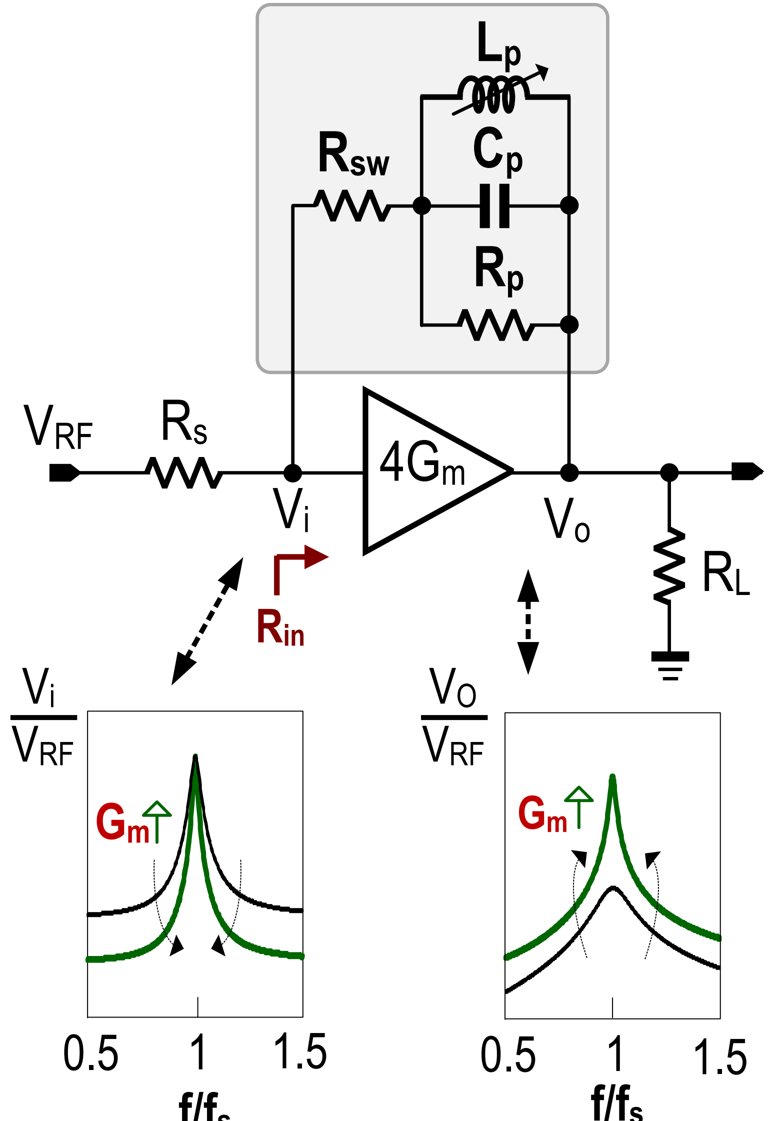
For input matching

$$R_{in} \approx \frac{R_{sw}}{4G_mR_L} + \frac{1}{4G_m} \text{ @ OB}$$

For OB blockers

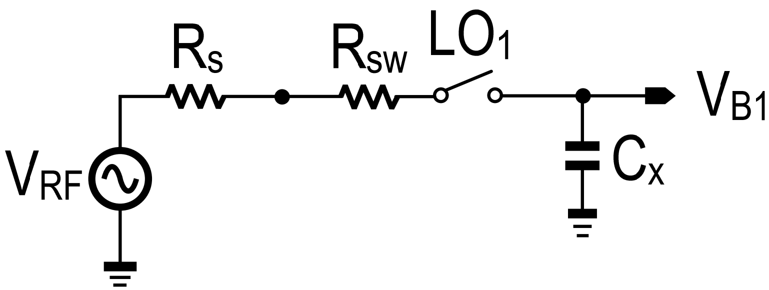
Ideally, when $4G_mR_{sw} = 0$

$V_o = 0$ (Infinity OB Rejection)

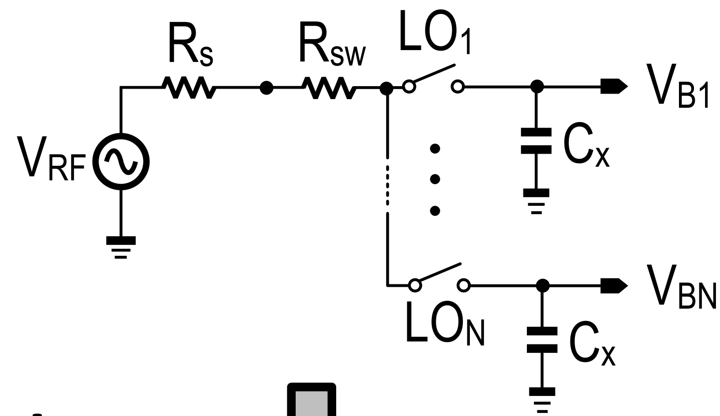


Gain-Boosted SC Networks

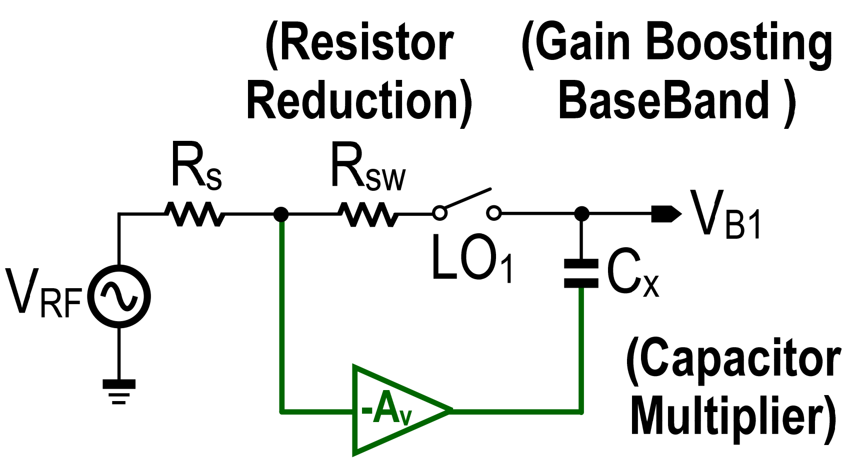
1-Phase SC Network

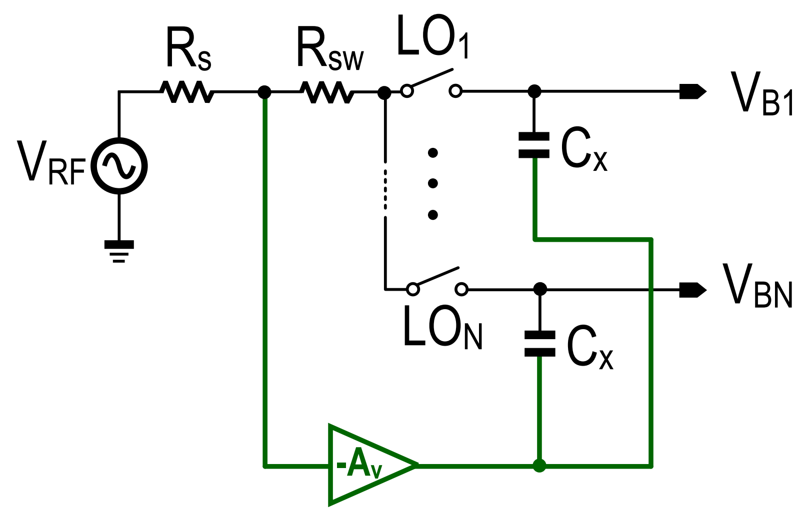


N-Phase SC Network

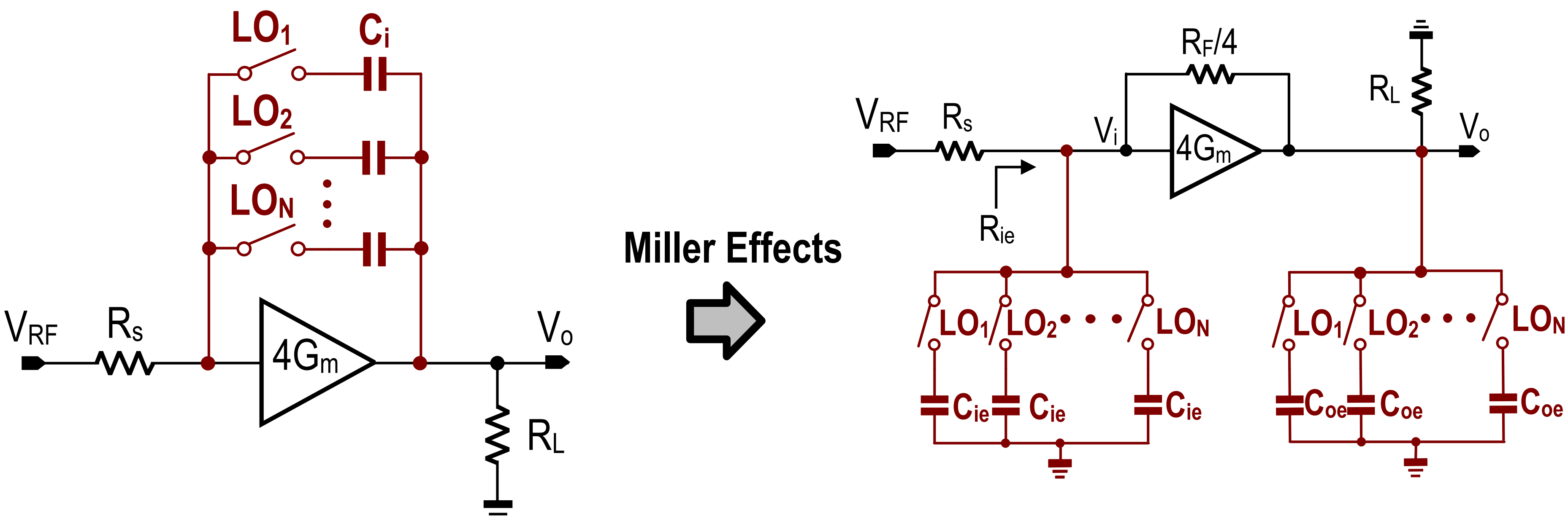


Gain Boosting by -A_v





Discrete-Time Miller Effect of N-Path LNA



Example :

R_F = 20 kΩ, R_L = 800 Ω, $4G_m$ = 20.55 mS

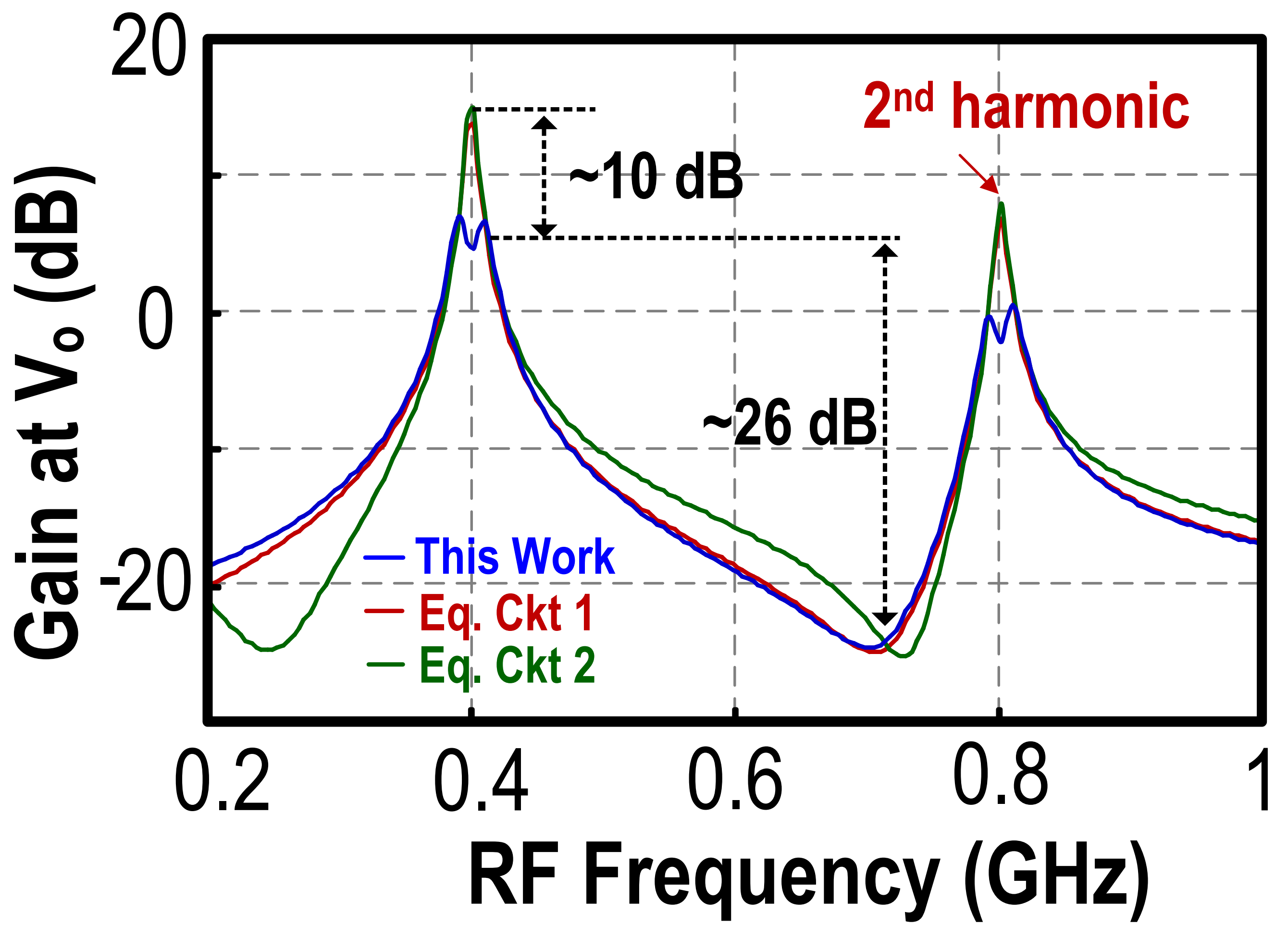
→ C_i = 12.5 pF and C_{ie} = 169 pF

$$C_{ie} \approx \left| \frac{(1 - G_m R_F) R_L}{R_L + R_F/4} \right| \times C_i$$

$$C_{oe} \approx C_i$$

☑ **Narrower BW achieved with small physical C_i**

Simulated Gain Response @ V_o

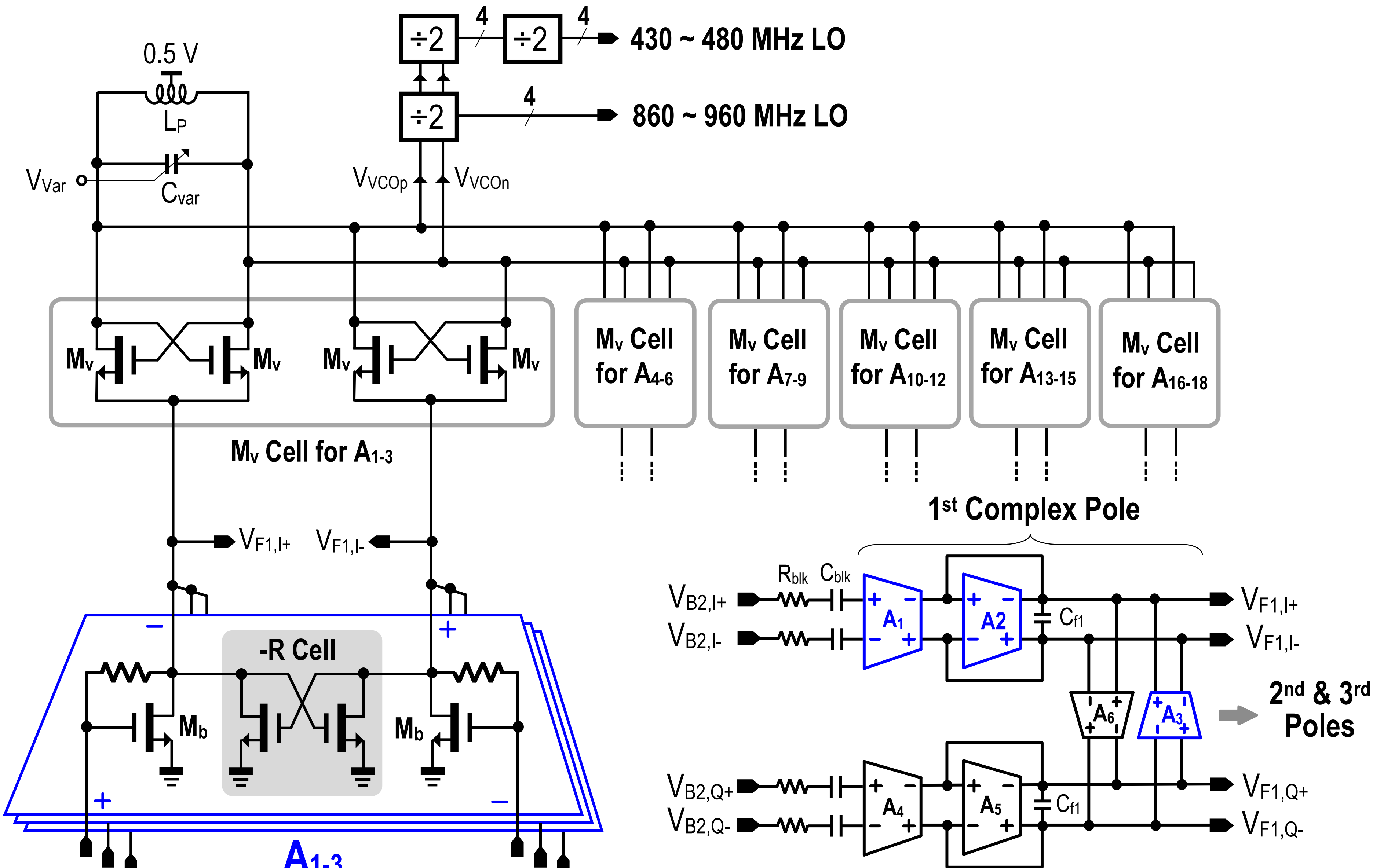


R_F = 20 kΩ
R_L = 800 Ω
R_s = 50 Ω
$4G_m$ = 20.55 mS
C_i = 12.5 pF
f_s = 400 MHz

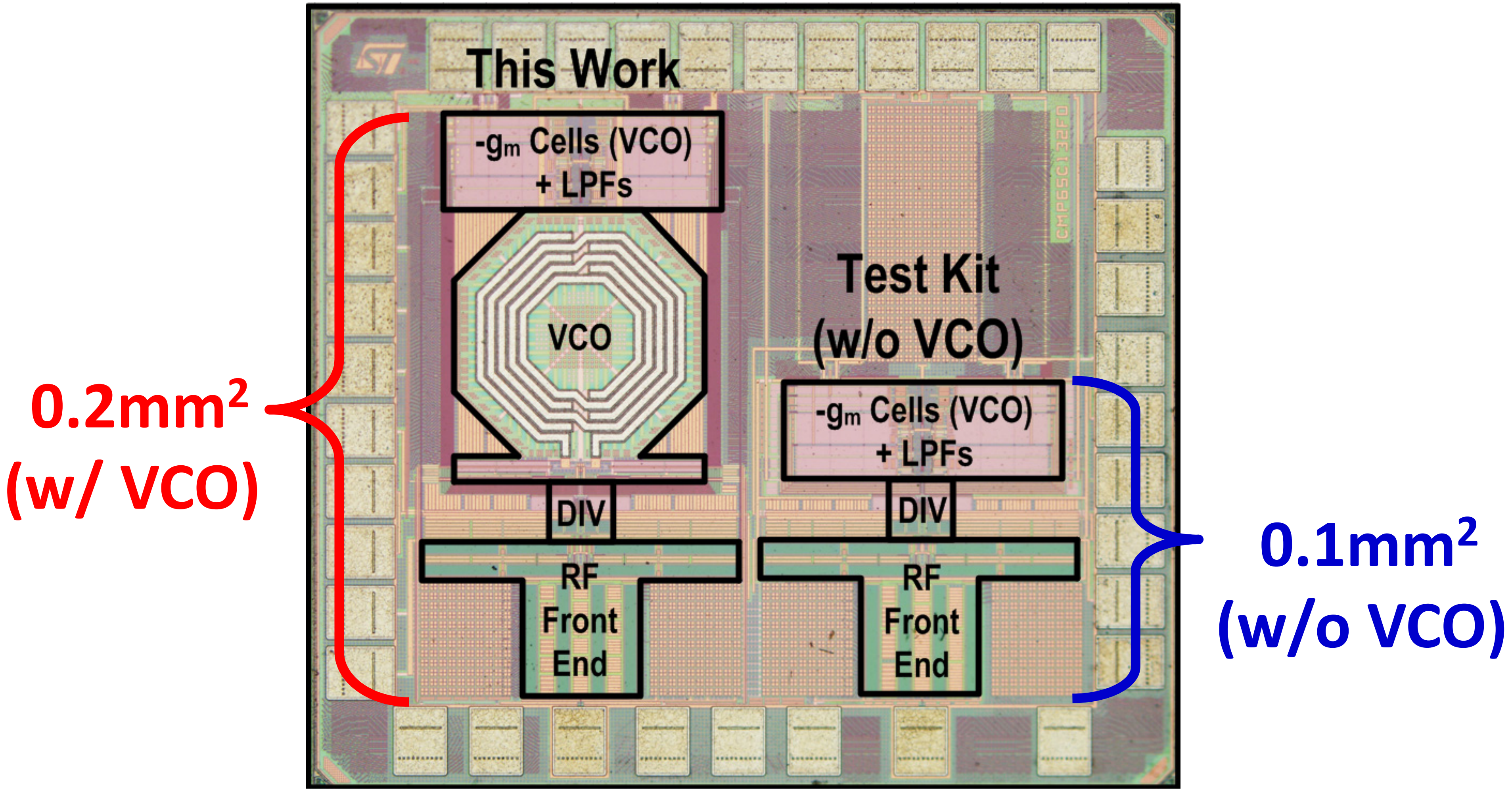
R_F should be relatively small to avoid too high BB gain

If $R_F \neq \infty$, This Work has more charge coupling (lower gain)

Current-reuse VCO-Filter and LO Gen.



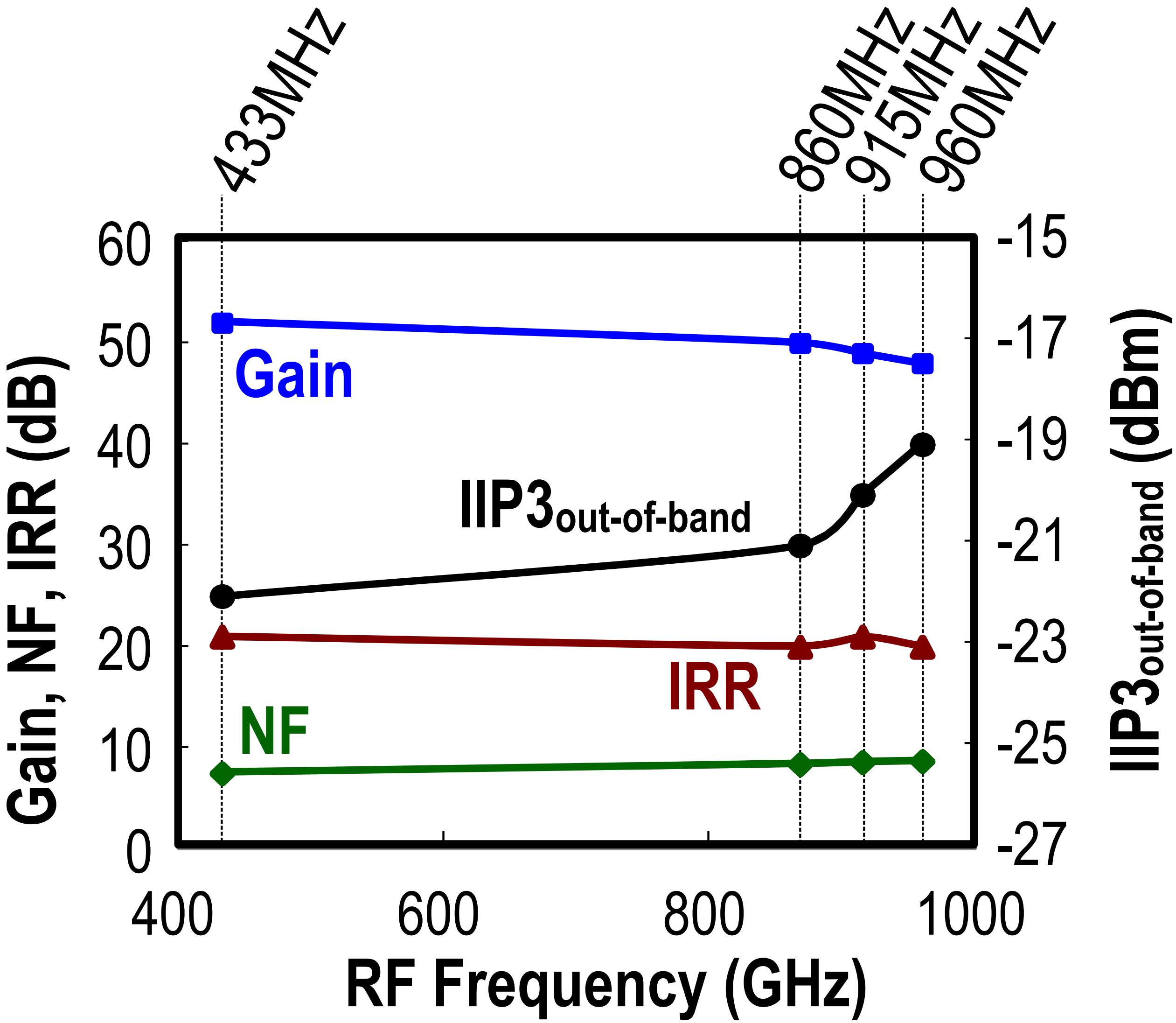
Chip Photo (65nm CMOS)



Capacitors in each design:

72pF MIMCAP (front-end) + 65pF MOMCAP (VCO-filter)

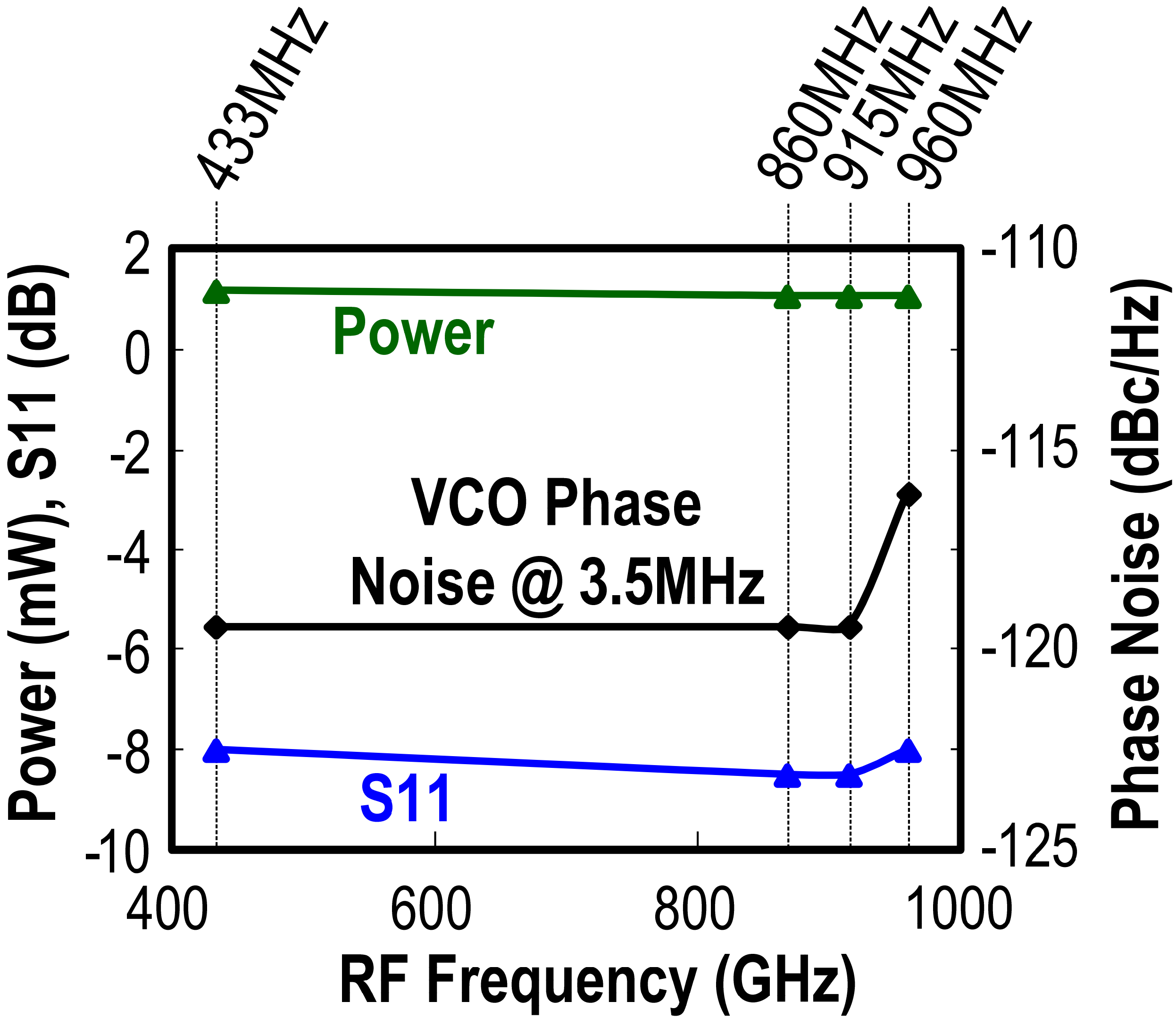
Measured Gain, IIP3, IRR and NF



433 to 960 MHz

- **RF-to-IF Gain**
  50 ± 2 dB
- **$IIP3_{out\text{-}of\text{-}band}$**
  -20.5 ± 1.5 dBm
- **IRR**
  20.5 ± 0.5 dB
- **NF**
  8.1 ± 0.6 dB

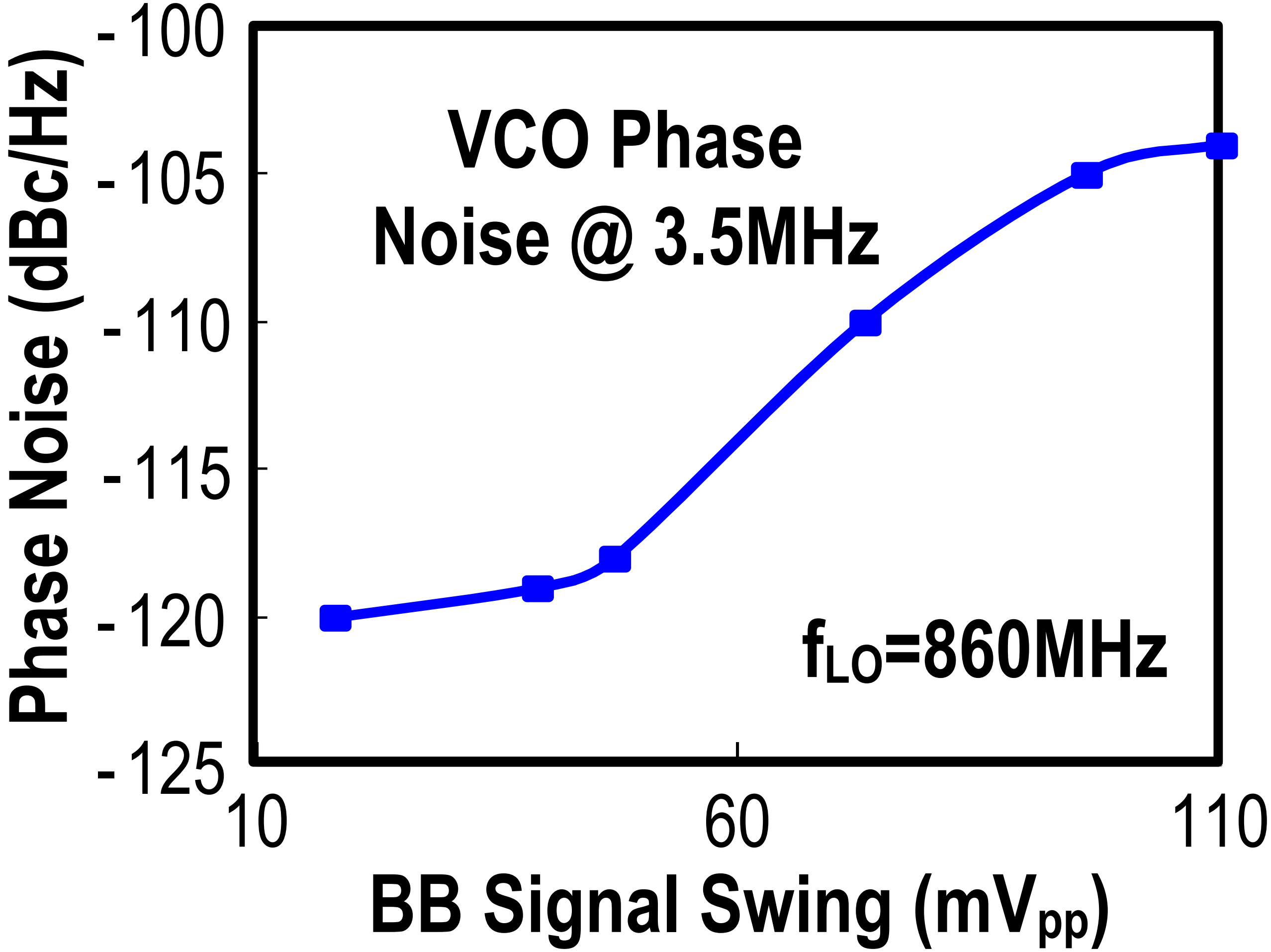
Measured Power, Phase Noise and S11



433 to 960 MHz

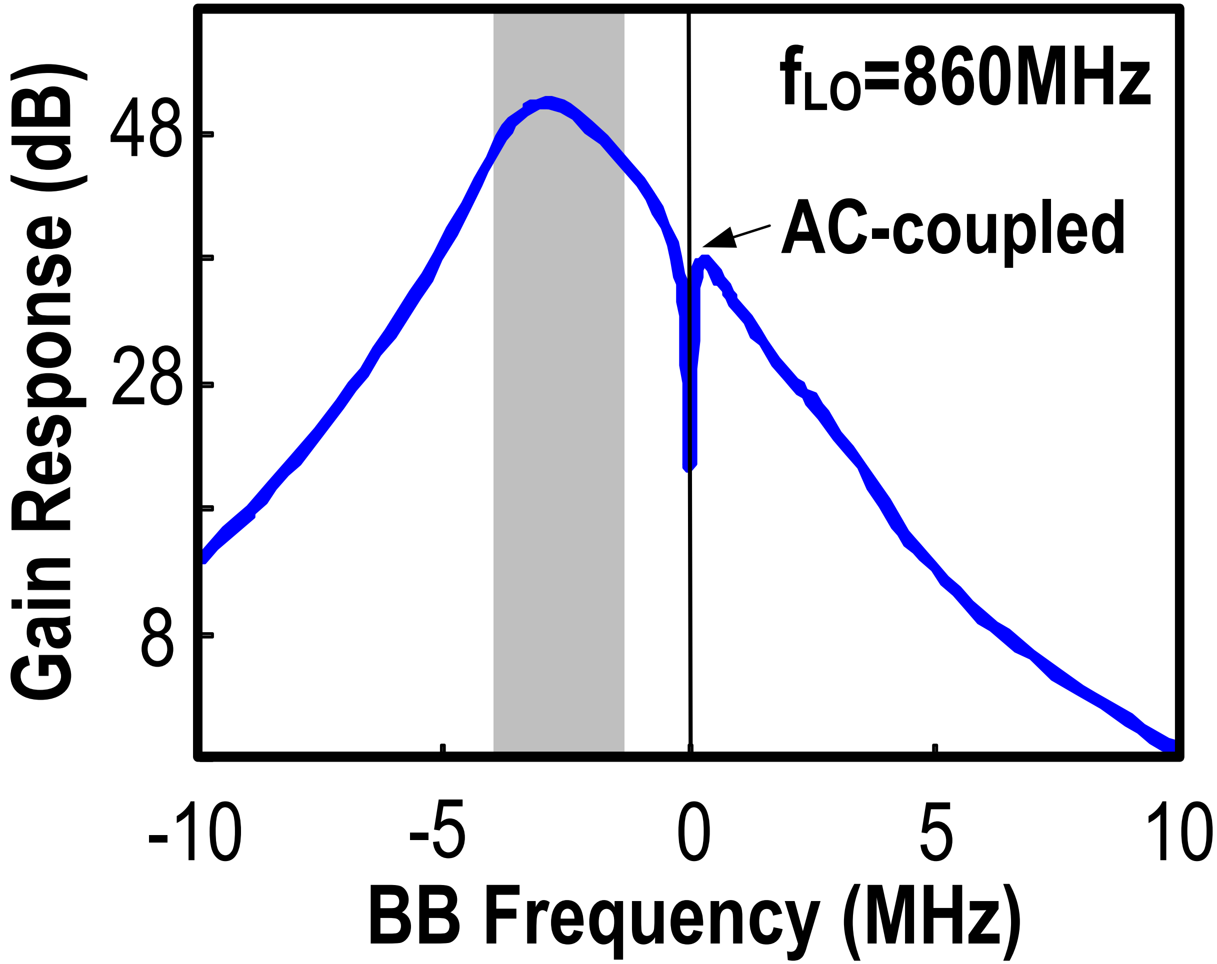
- **Power**
  1.15 ± 0.05 mW
- **VCO PN**
  -117.4 ± 1.7 dBc/Hz @ 3.5MHz
- **S11**
  <-8 dB

VCO Phase Noise vs. BB Signal Swing



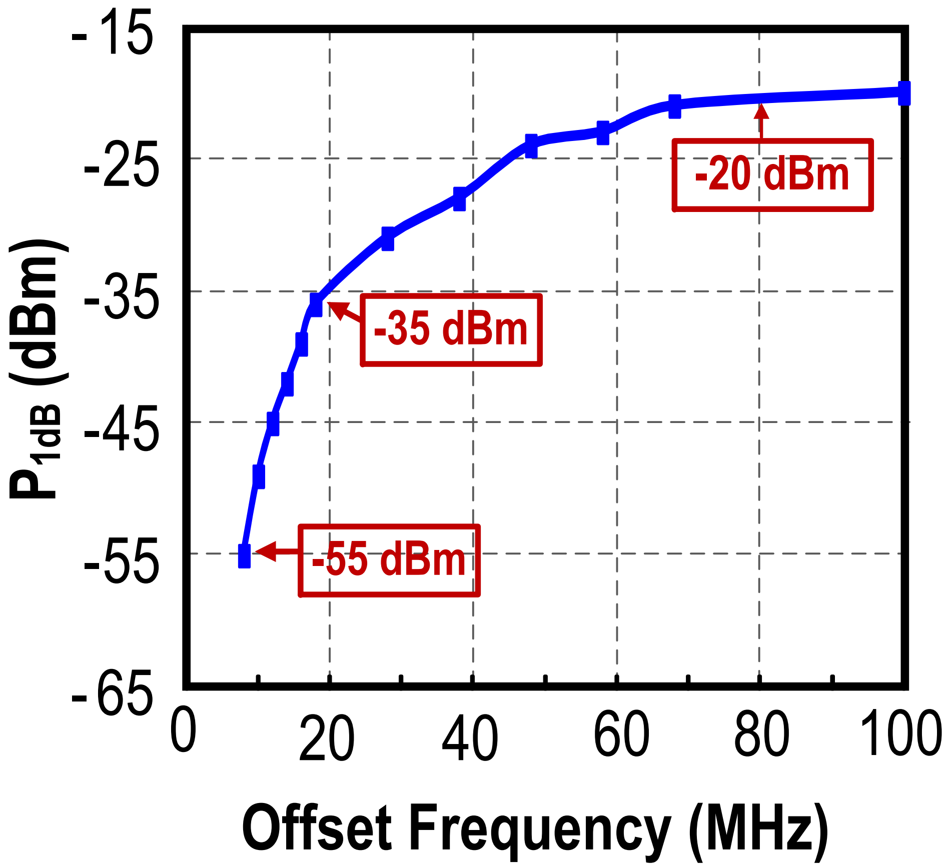
- Current-reuse VCO-filter: the BB signal swing affects the phase noise due to finite isolation

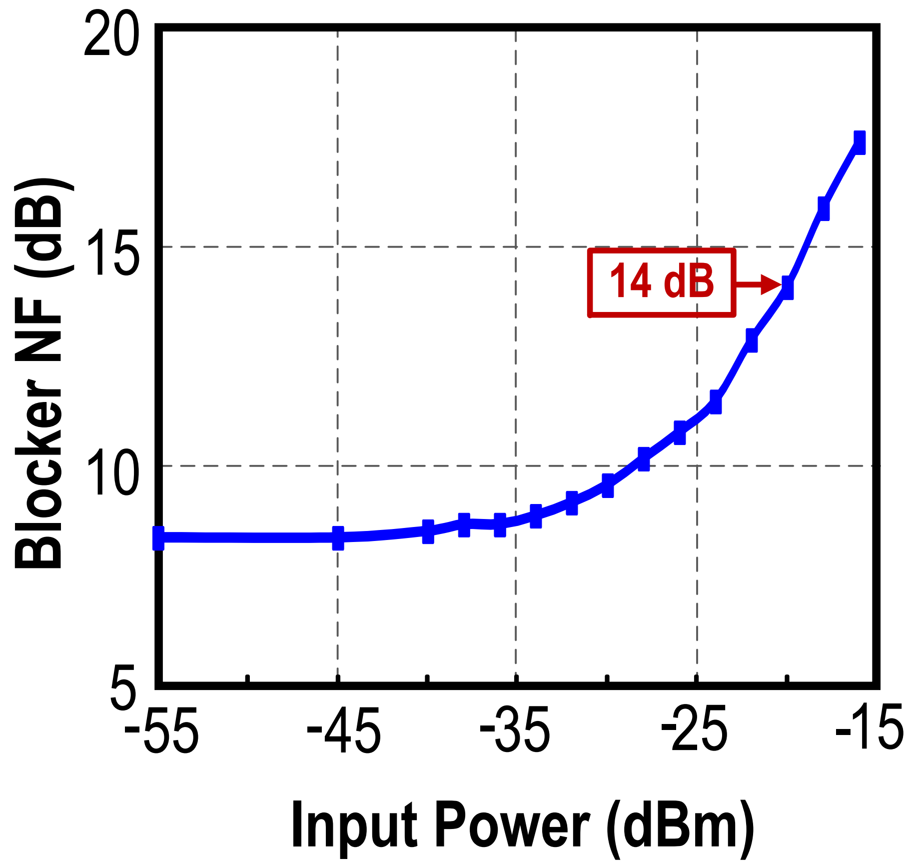
Complex Low-IF Gain Response



- 24 dB first channel rejection @ 5 MHz offset
- 41 dB adjacent rejection @ 10 MHz offset

Measured P_{1dB} and Blocker NF





- **P_{1dB}: -20 dBm @ 80 MHz**
- **Blocker NF: 14 dB @ 1-tone blocker of -20 dBm at 50 MHz offset**

Comparison with the State-of-the-Art

	This Work	ISSCC'13 [1] (w/ VCO)	ISSCC'13 [2]	JSSC'10 [6]
Application	**433/860/915/960 MHz (ZigBee/IEEE802.15.4)**	2.4 GHz (ZigBee/ IEEE 802.15.4)	2.4 GHz (Energy Harvesting)	2.4 GHz (ZigBee/ IEEE 802.15.4)
BB Filter	3 complex poles	1 Biquad, 4 complex poles	2 real poles	3 complex poles
Input Matching Technique	**On-chip N-path SC (tunable by LO, high Q)**	On-chip LC (fixed, low Q)	Off-chip LC (fixed, low Q)	Off-chip LC (fixed, high Q)
External Components	**zero**	zero	2 caps, 1 inductor	1 caps, 1 inductor
Input Matching BW and Tunability	**433 to 960 MHz (tunable by LO)**	2.25 to 3.55 GHz (fixed)	~ 2 to 2.6 GHz (fixed)	2.3 to 2.6 GHz (fixed)
Active Area (mm^2)	**0.2**	0.3	2.5	0.35
Power (mW) @ V_{DD}	**1.15 ± 0.05 @ 0.5 V**	2.7 @ 0.6/1.2 V	1.6 @ 0.3 V	3.6 @ 1.2 V
Gain (dB)	50 ± 2	55	83	75
NF (dB)	8.1 ± 0.6	9	6.1	9
$IIP3_{out\text{-}of\text{-}band}$ (dBm)	-20.5 ± 1.5	–6	–21.5	–12.5
IRR (dB)	20.5 ± 0.5	28	N/A	35
VCO PN (dBc/Hz)	-117.4 ± 1.7 @ 3.5 MHz	–115 @ 3.5 MHz	–112 @ 1 MHz	–116 @ 3.5 MHz
Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS	90 nm CMOS

Conclusions

A sub-GHz multi-ISM-band ZigBee receiver is demonstrated. It features:

- ☑ **Function-Reuse Front-End** - to recycle the power between the RF and BB amplifiers
- ☑ **Gain-Boosted 4-Path SC Branch** - to assist the input impedance matching and RF filtering
- ☑ **Current-Reuse VCO-Filter** - to save power at a low V_{DD} of 0.5V

Multi Bands, Lowest Power, Smallest Area and Zero External Components

Acknowledgements

- Multi-Year Research Grant of University of Macau
- Macao Science and Technology Development Fund (FDCT)

A 1.2nJ/bit 2.4GHz Receiver with A Sliding-IF Phase-to-digital Converter for Wireless Personal/Body Area Networks

Yao-Hong Liu, Ao Ba, J.H.C. van den Heuvel, Kathleen Philips, Guido Dolmans, Harmke de Groot

IMEC-Holst Centre, Eindhoven, The Netherlands

Holst Centre

Open Innovation by IMEC and TNO

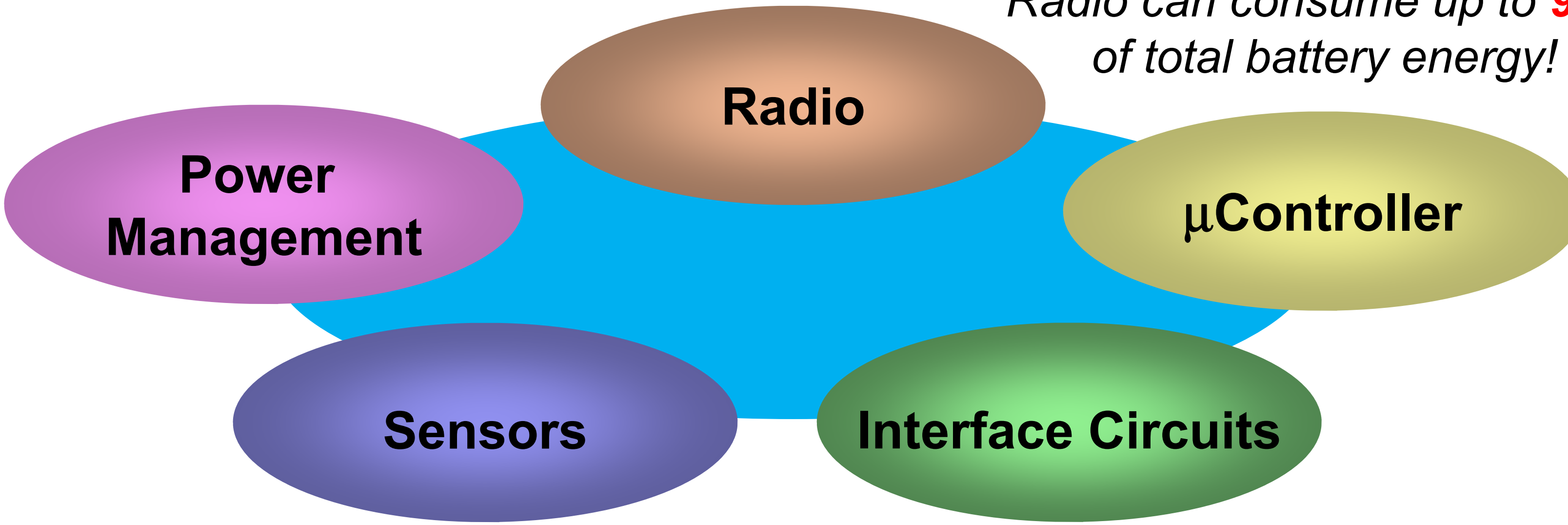
imec

Outline

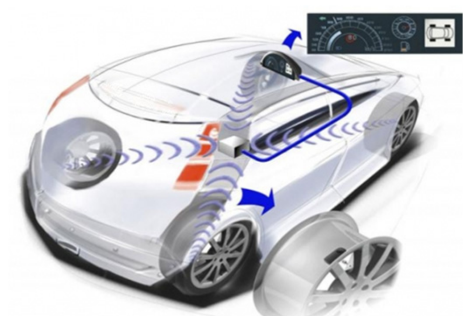
- Introduction
- Phase-domain FSK/PSK RXs
- Circuit implementation
- Measurement results
- Conclusion

Wireless Sensors in Personal/Body Area Networks

Radio can consume up to ***90%*** *of total battery energy!*



Healthcare **Automotive** **Smart Buildings**



Short-range Standards in 2.4GHz ISM for WPAN/BANs

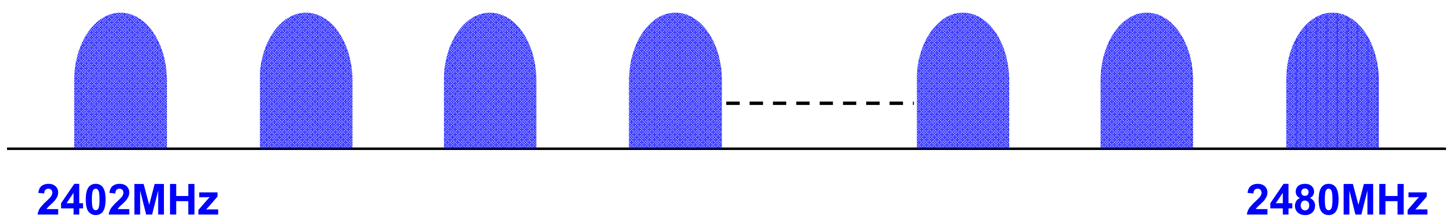
Bluetooth Smart
Mod: GFSK

ZIgBee
IEEE 802.15.4
Mod.: HS-OQPSK

Bluetooth®

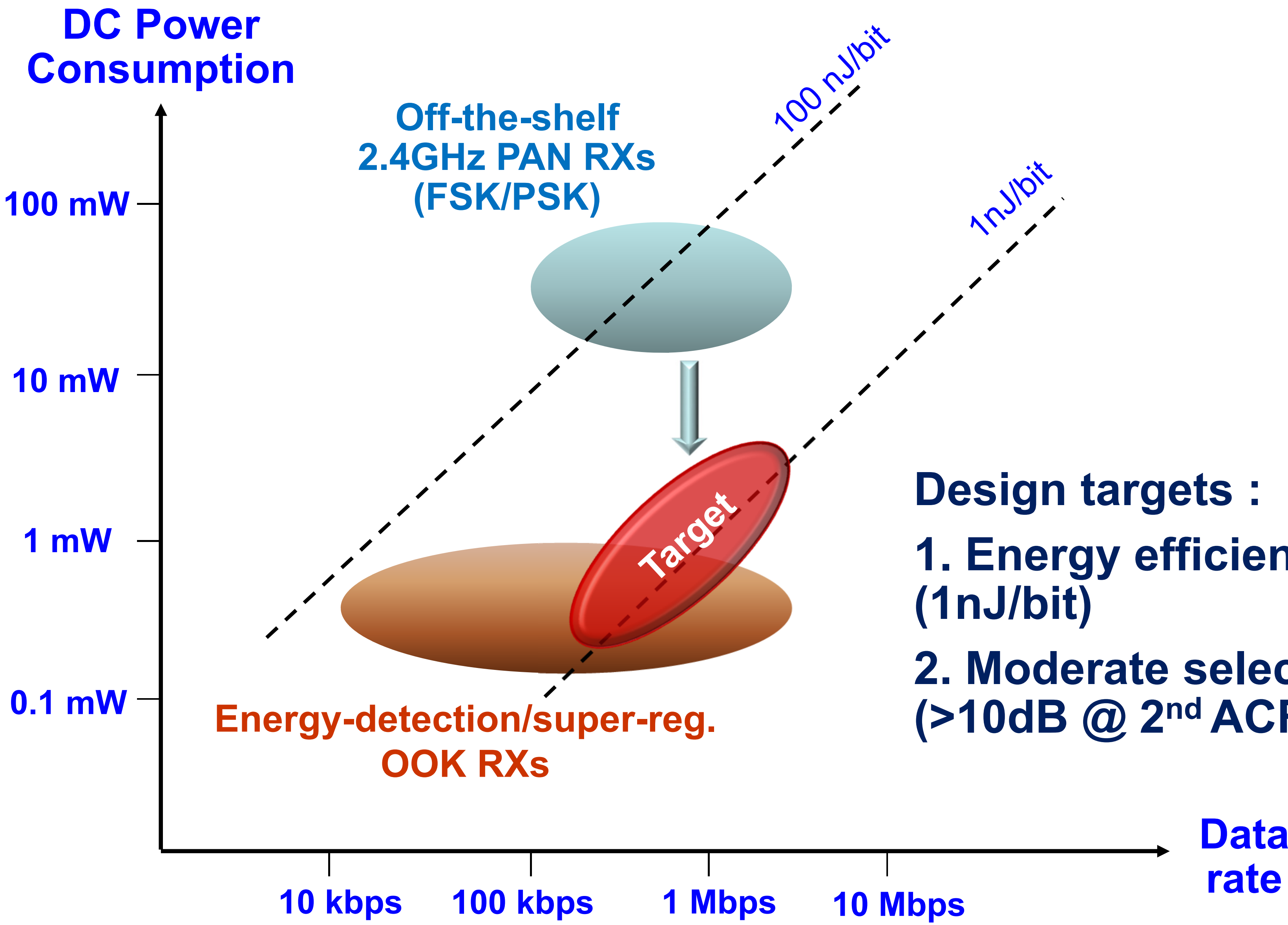
ZigBee®
Control your world

Bluetooth Smart channels



- The 2.4GHz ISM RXs should have sufficient selectivity
  - Co-existence of short-range standards
  - Up to 40 wireless sensors operated in same network

Design Targets



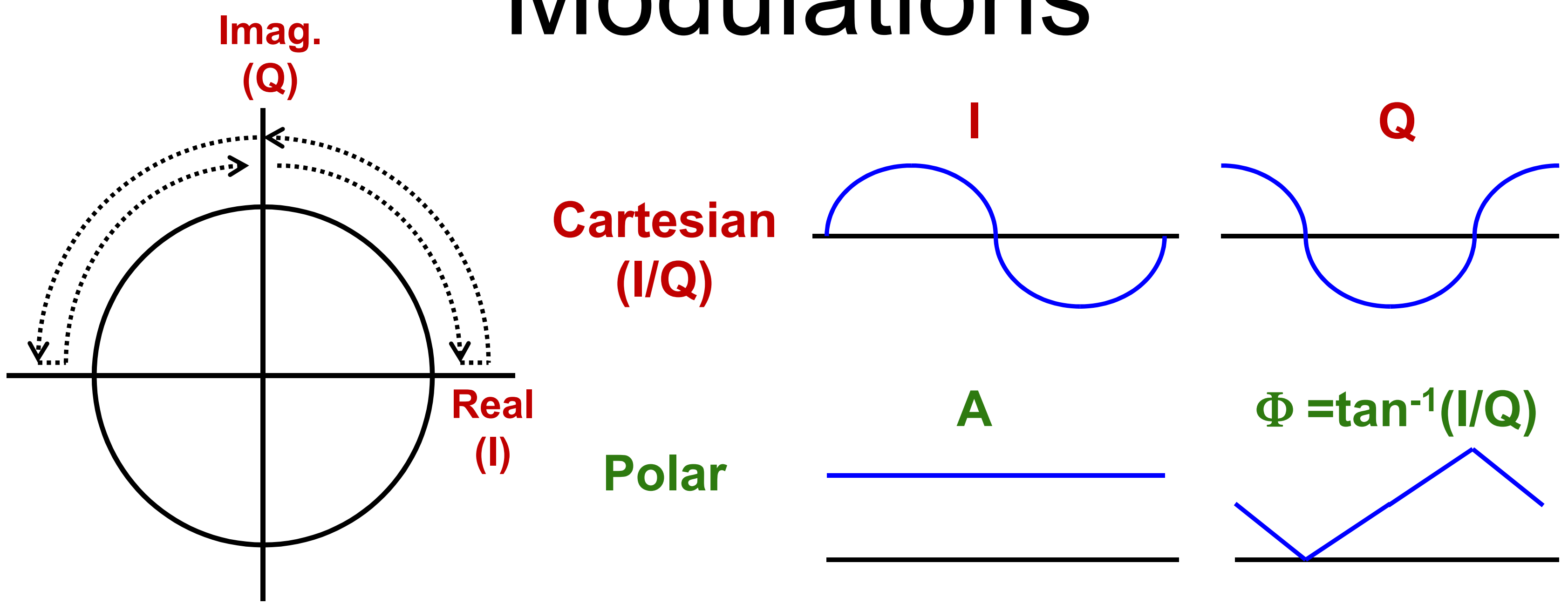
Design targets :

1. **Energy efficient (1nJ/bit)**
2. **Moderate selectivity (>10dB @ 2nd ACR)**

Outline

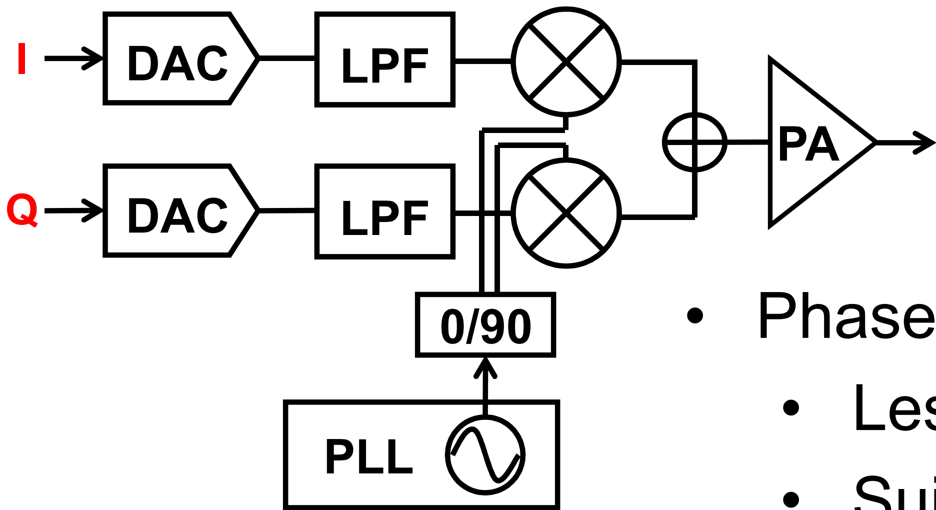
- Introduction
- Phase-domain FSK/PSK RXs
- Circuit implementation
- Measurement results
- Conclusion

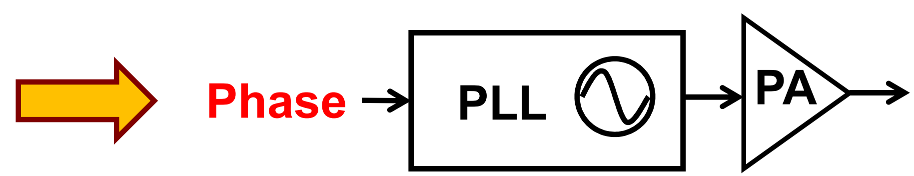
Constant-envelope FSK/PSK Modulations



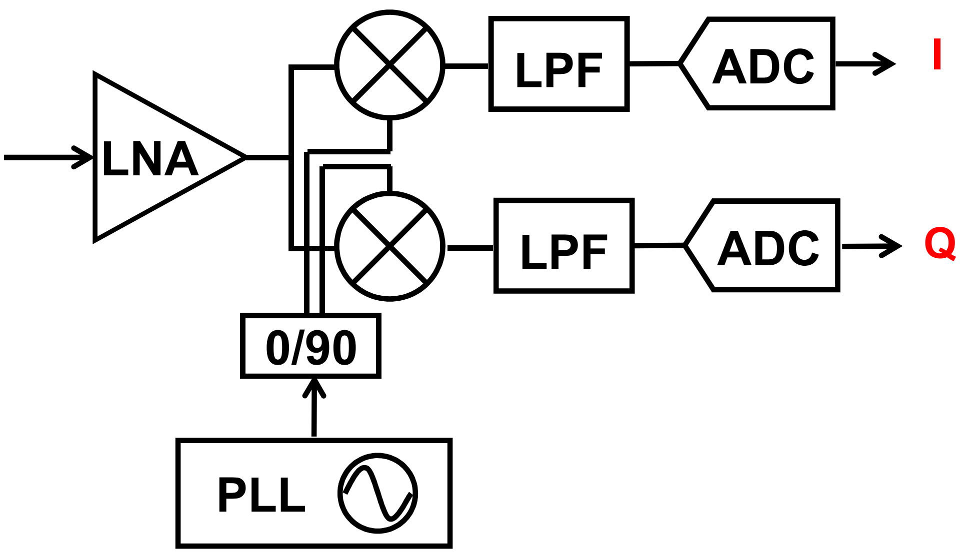
- Constant-envelope modulations are suitable for low power implementation
  - RF hardware can be simplified from “2D” to “1D”
  - Analog circuits can be driven into saturation mode to enhance efficiency

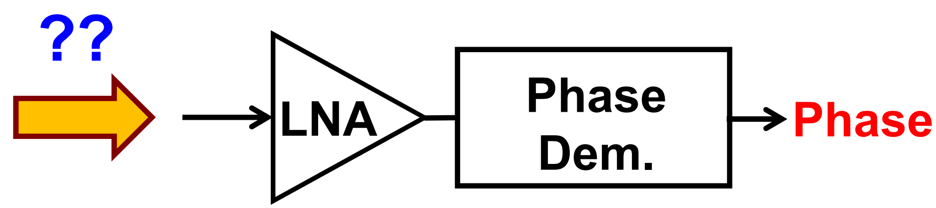
Phase-domain Transceivers





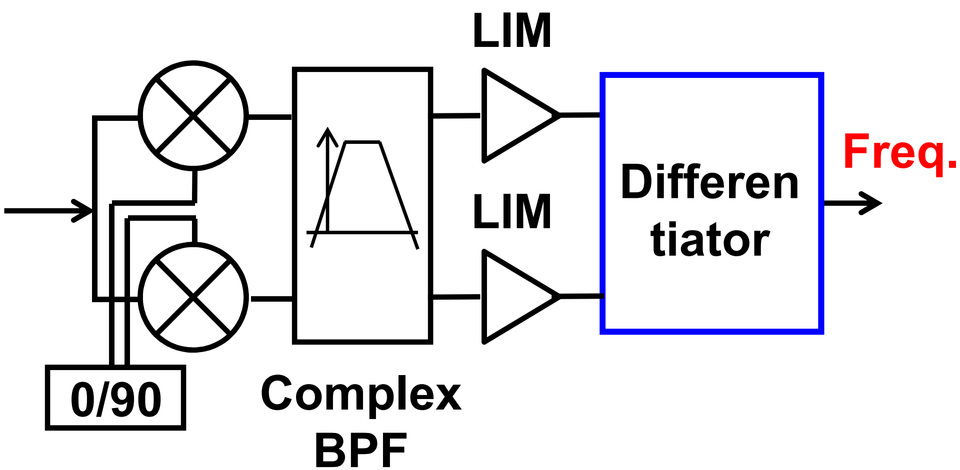
- Phase-domain PLL-based TXs
  - Less restricted by supply
  - Suitable for technology scaling





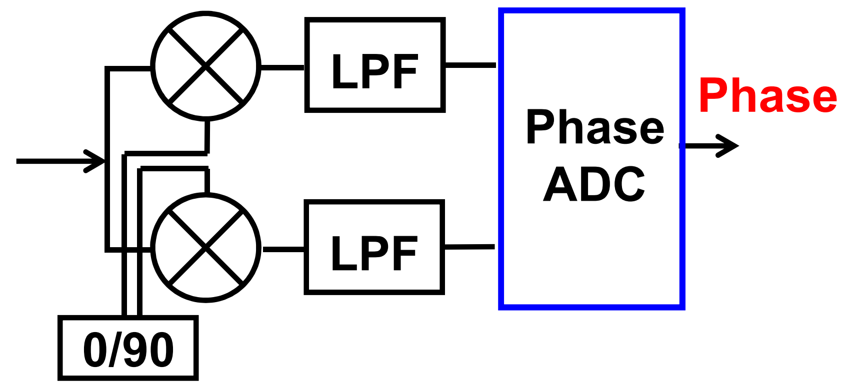
Differentiator and Phase-ADC-based FSK/PSK RXs

Differentiator-based FSK RX



[Darabi, JSSC', Dec., 2001]

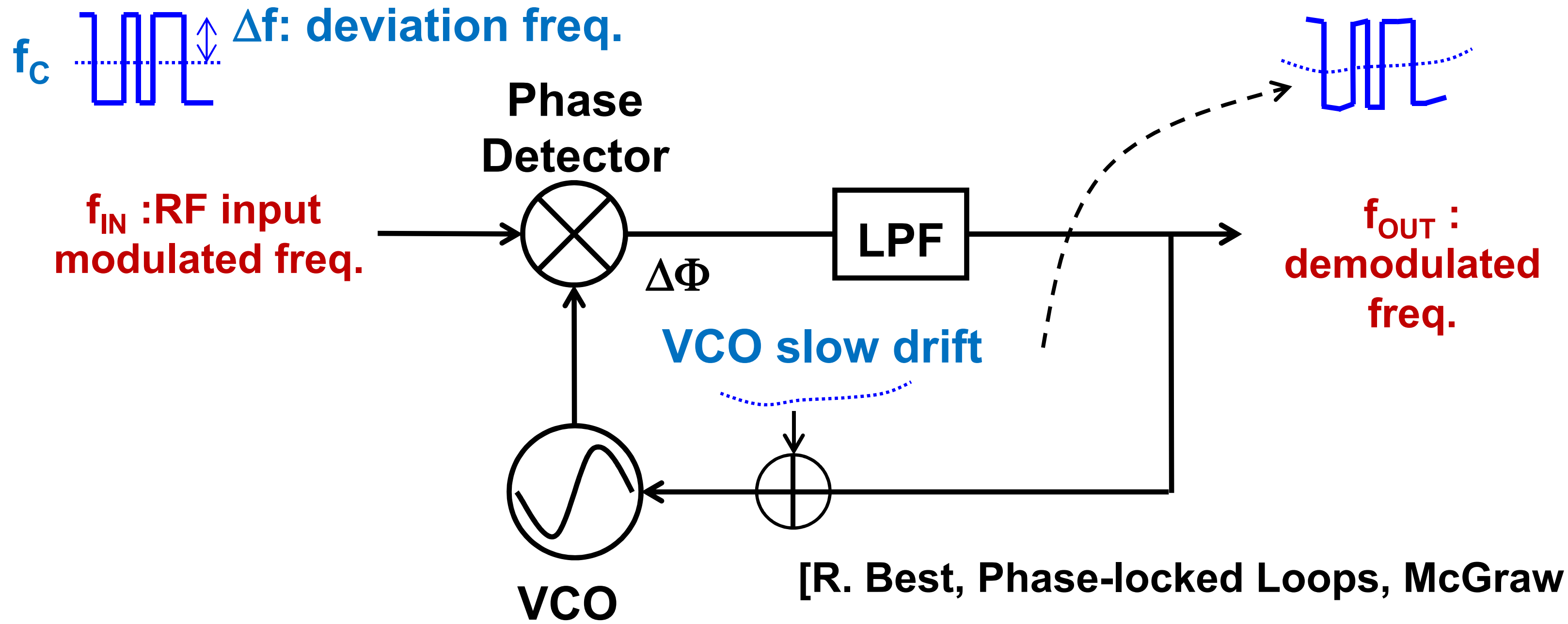
Phase-ADC-based FSK/PSK RX



[Masuch, MTT', Apr. , 2013]

- Use a differentiator or a phase ADC to replace I/Q ADCs
- Still require I/Q mixers and high-freq. quad.-LO gen

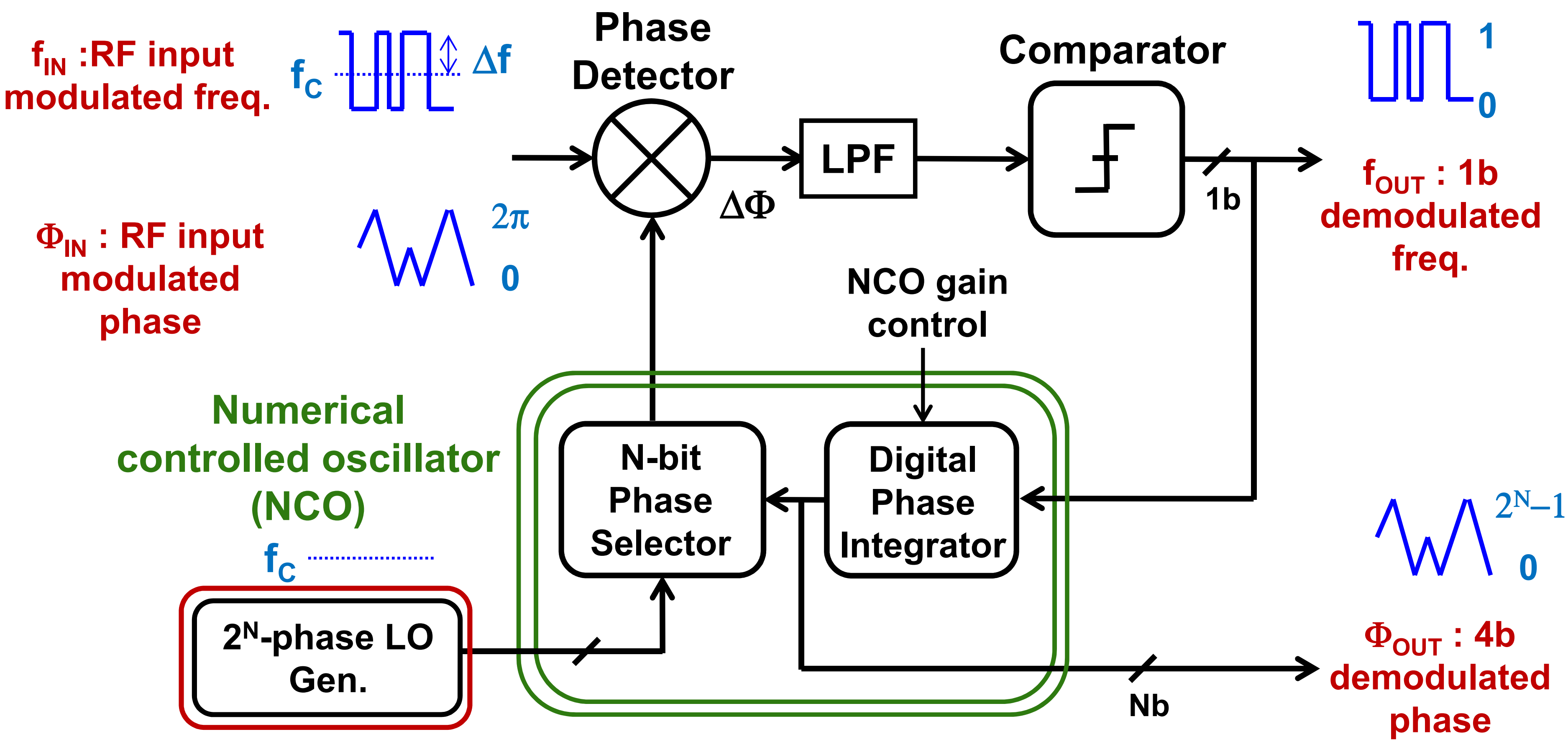
Phase-tracking RX



[R. Best, Phase-locked Loops, McGraw Hill]

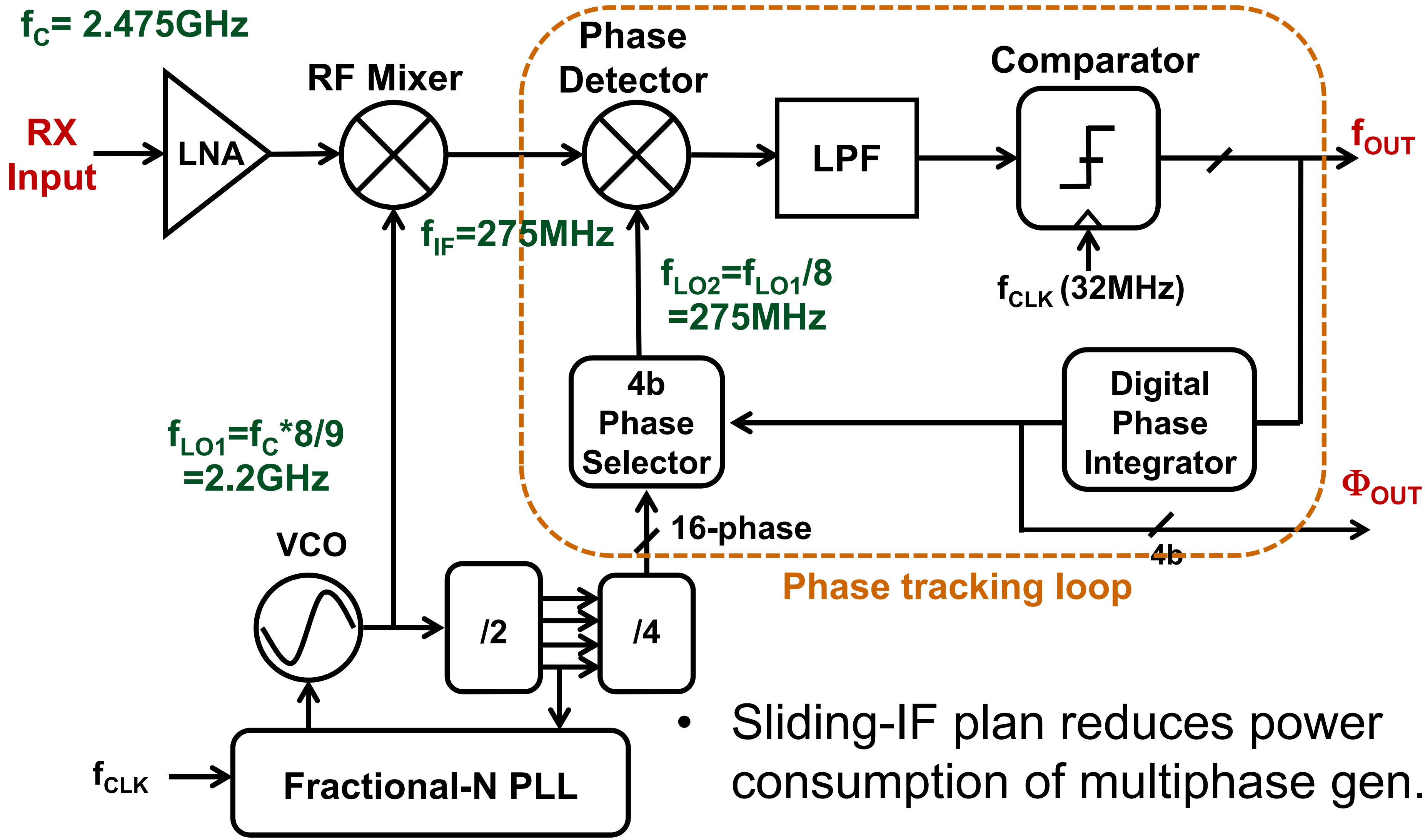
- The phase-tracking RXs (1) recover the carrier f_C, and (2) track the modulated frequency (Δf) or phase
- The RX might track to interference but desired signal
- VCO close-in phase noise translates to output low-freq. noise

Phase Tracking RX Using Multi-phase Selection



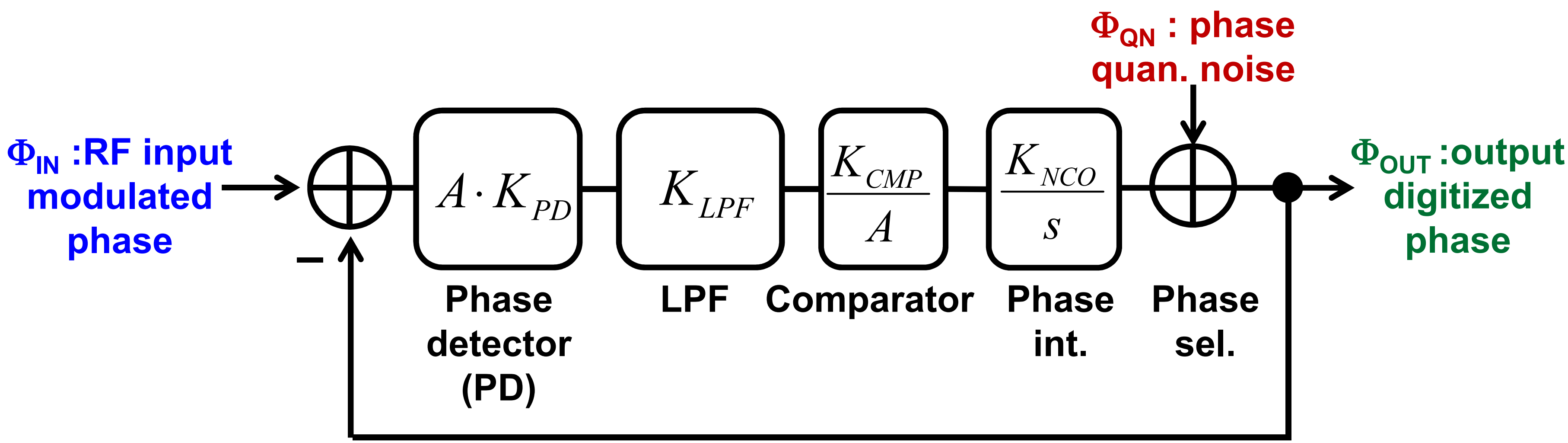
The 2.4GHz multi-phase LO generation is power hungry!

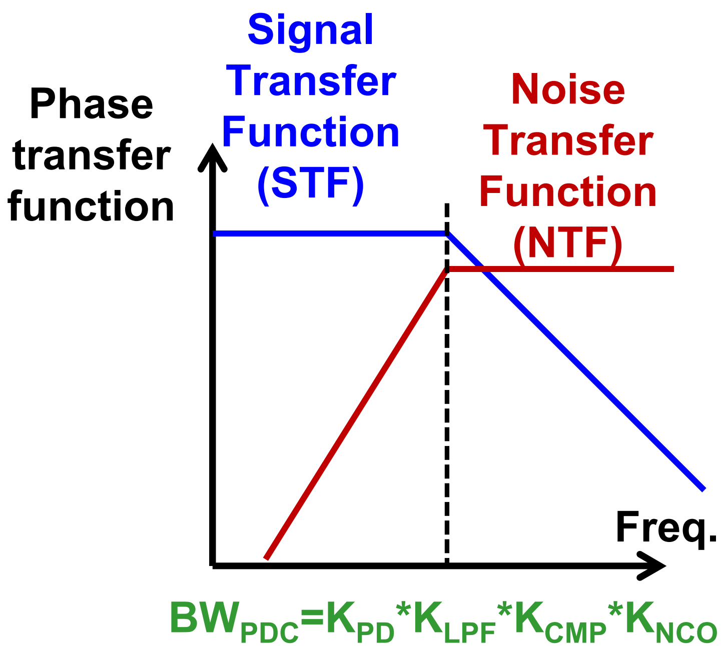
Sliding-IF Phase-to-digital Converter (SIF-PDC)



- Sliding-IF plan reduces power consumption of multiphase gen.

Phase-Domain Freq. Response

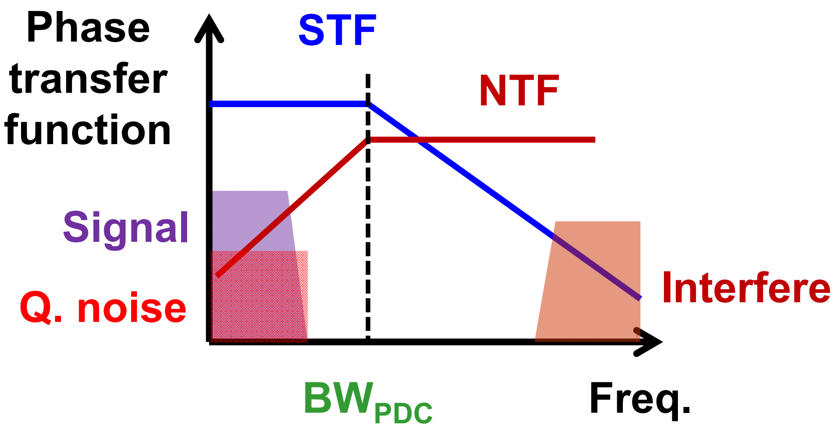


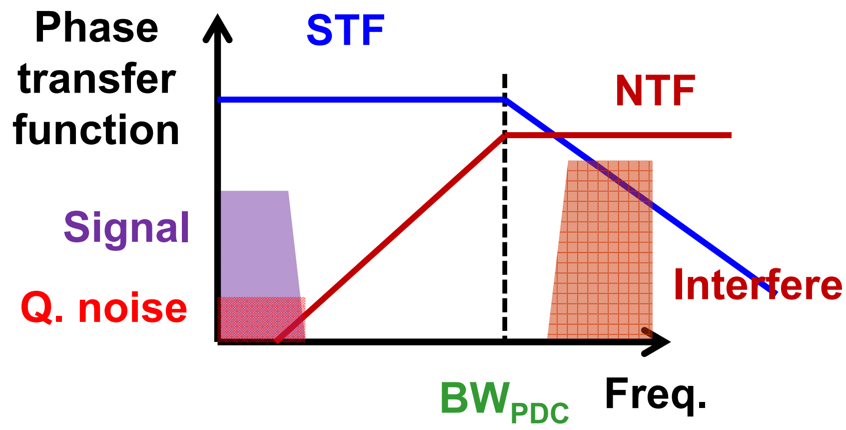


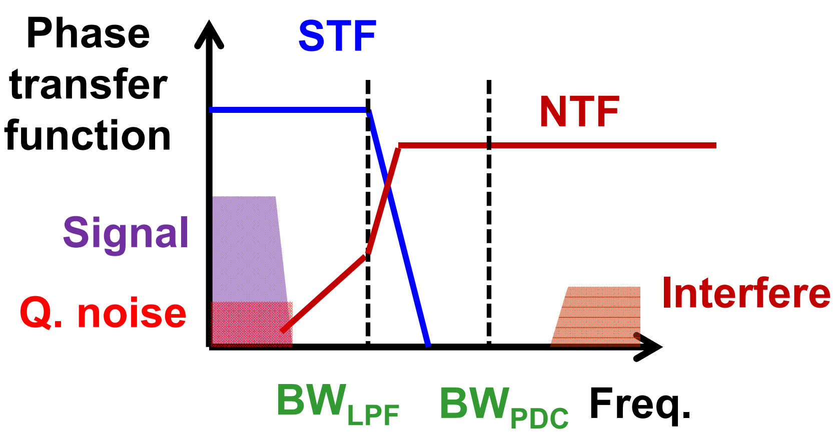
A: signal amplitude
K_{PD}: phase detector gain
K_{LPF}: LPF gain
K_{CMP}: comparator scaling factor
K_{NCO}: phase integrator gain

- Low-pass STF (Φ_{OUT}/Φ_{IN}): suppress out band interference
- High-pass NTF (Φ_{OUT}/Φ_{QN}) : relax phase resolution ($\Sigma\Delta$)

Bandwidth Selection



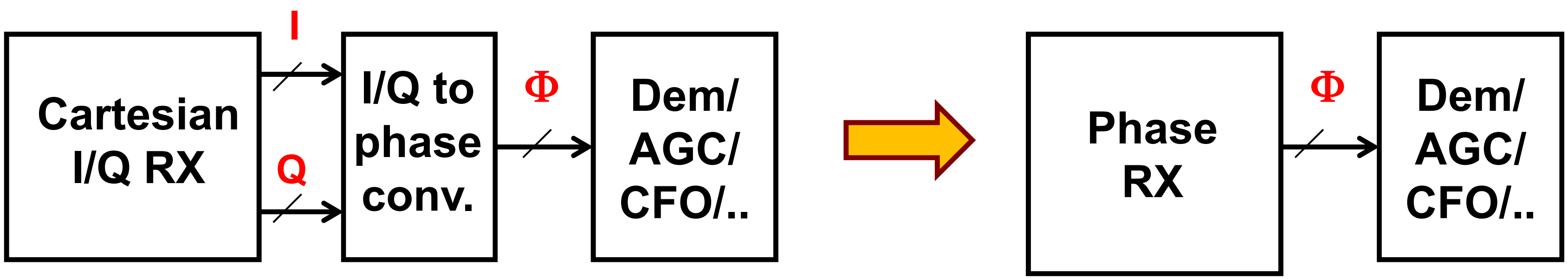




- Low BW_{LPF} ➔ interference rejection
- High BW_{PDC} ➔ relax phase resolution

Digital Baseband for SIF-PDC

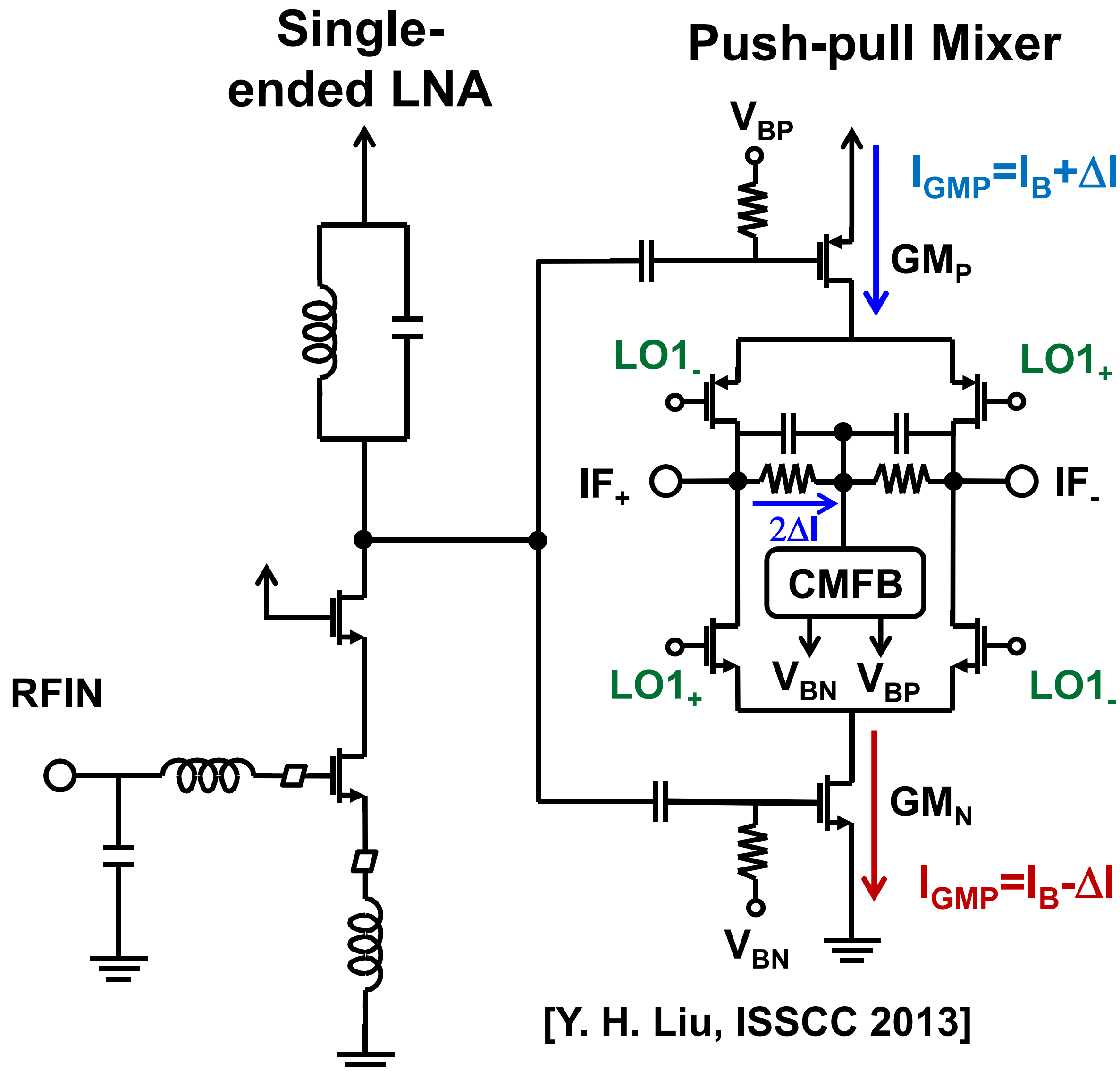
- Phase-domain RXs simplify digital baseband design
  - I/Q to phase conversion is not needed
  - Relaxed auto gain control (AGC)
  - Simple carrier freq. offset (CFO) detection and compensation



Outline

- Introduction
- Phase-domain FSK/PSK RXs
- Circuit implementation
- Measurement results
- Conclusion

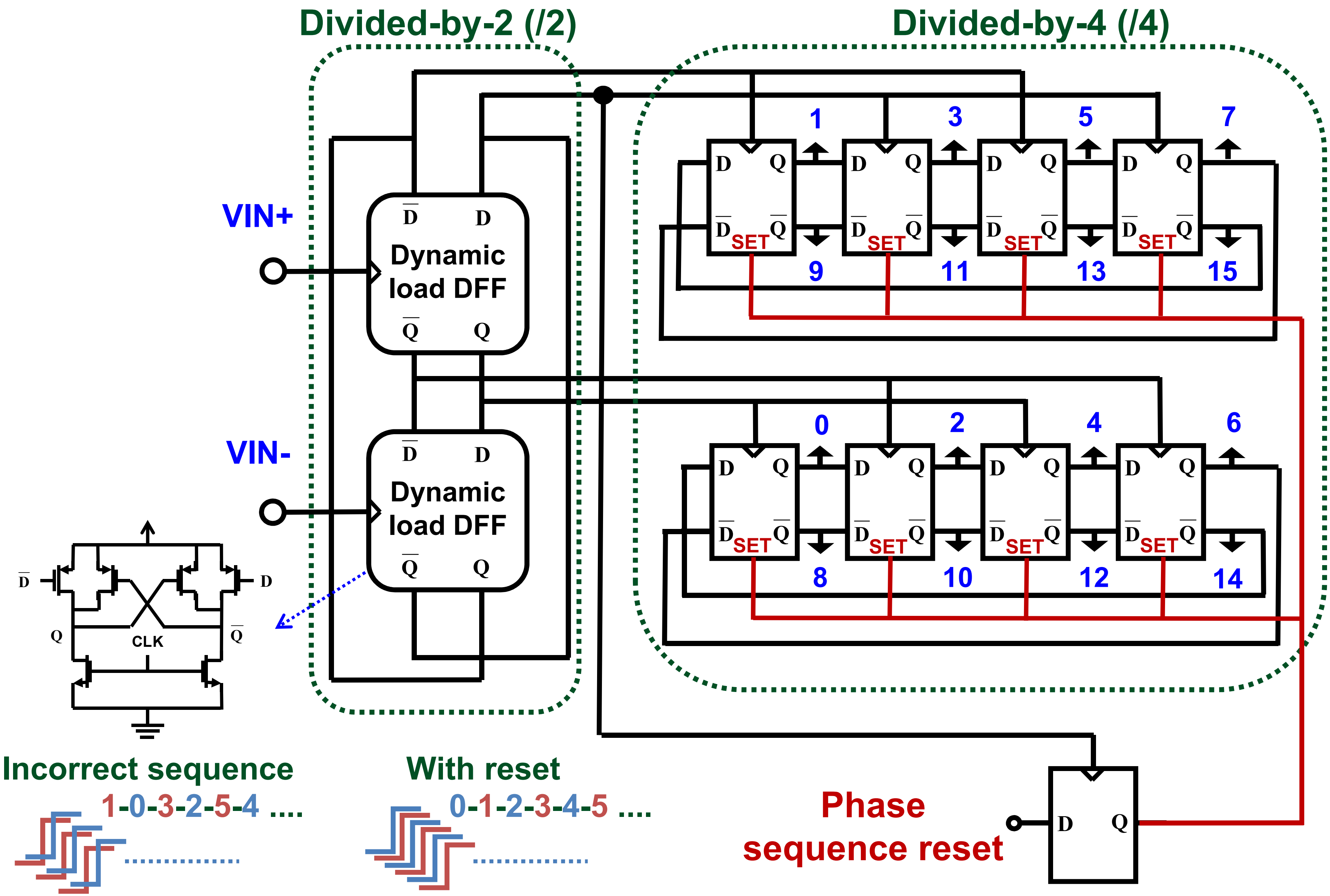
RX Front-end



[Y. H. Liu, ISSCC 2013]

- Singe-ended LNA: avoid balun and low power consumption
- Push-pull mixer: better gm efficiency and noise performance
- 1mW @ 1V supply
- 5dB NF

Divider and Multi-phase Gen.



Outline

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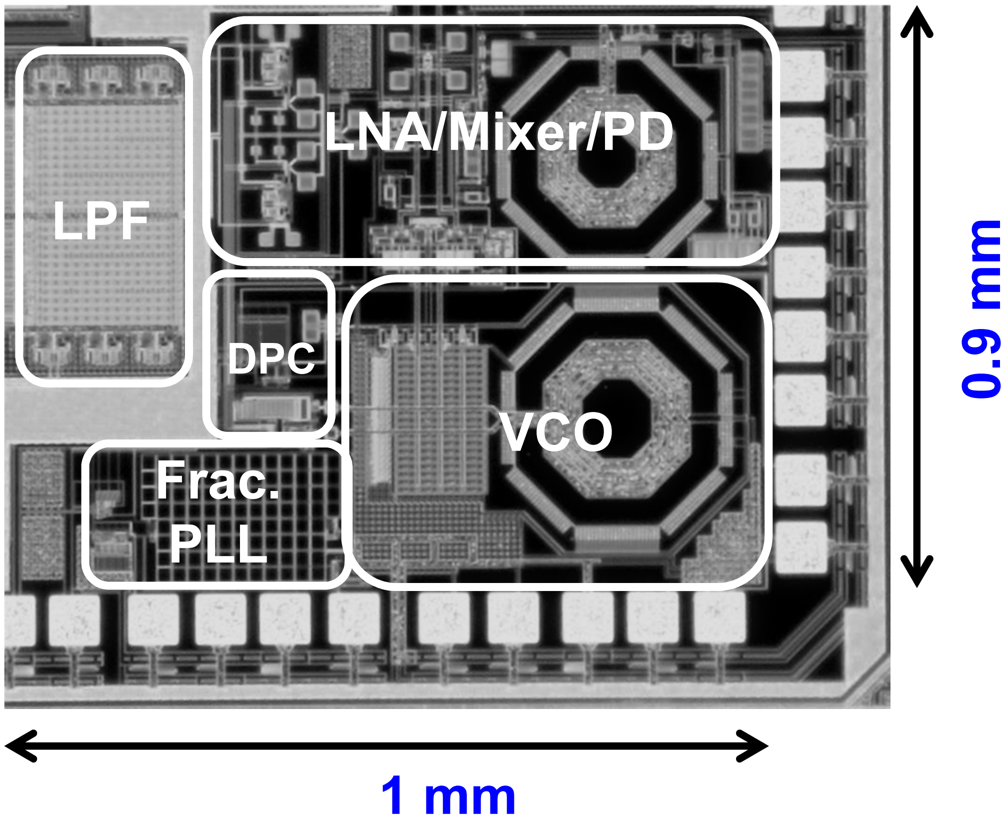
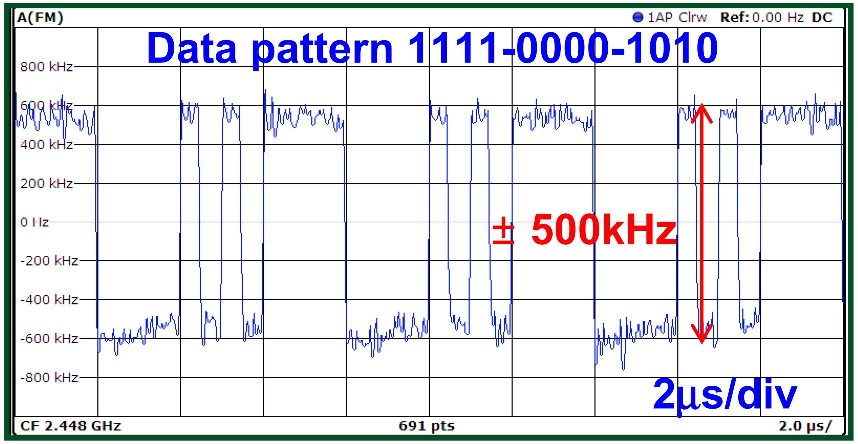
Chip Photo



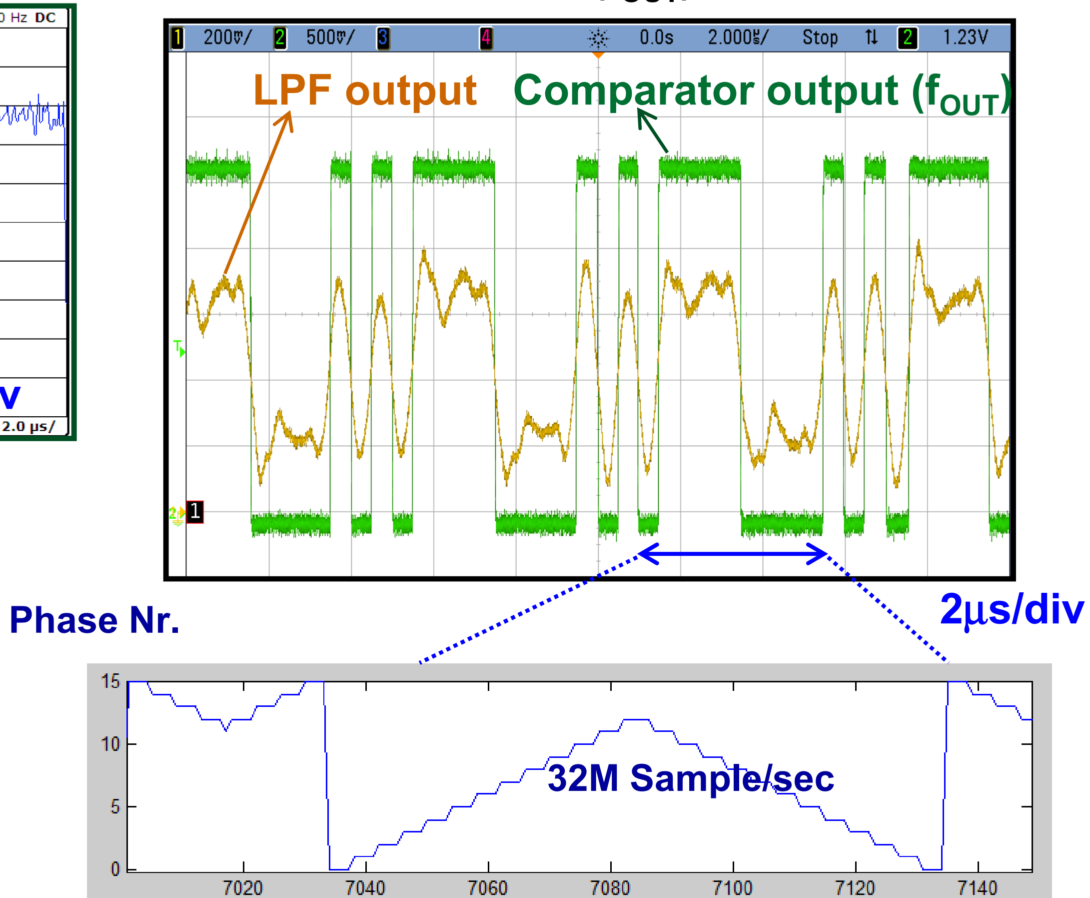
- TSMC 90-nm CMOS
- Core analog active area: 0.9 mm^2
- Saves around 25% area compared to conventional sliding-IF I/Q RXs

2-Mbps HS-OQPSK Demodulated Waveform

TX frequency deviation @ 2.45GHz



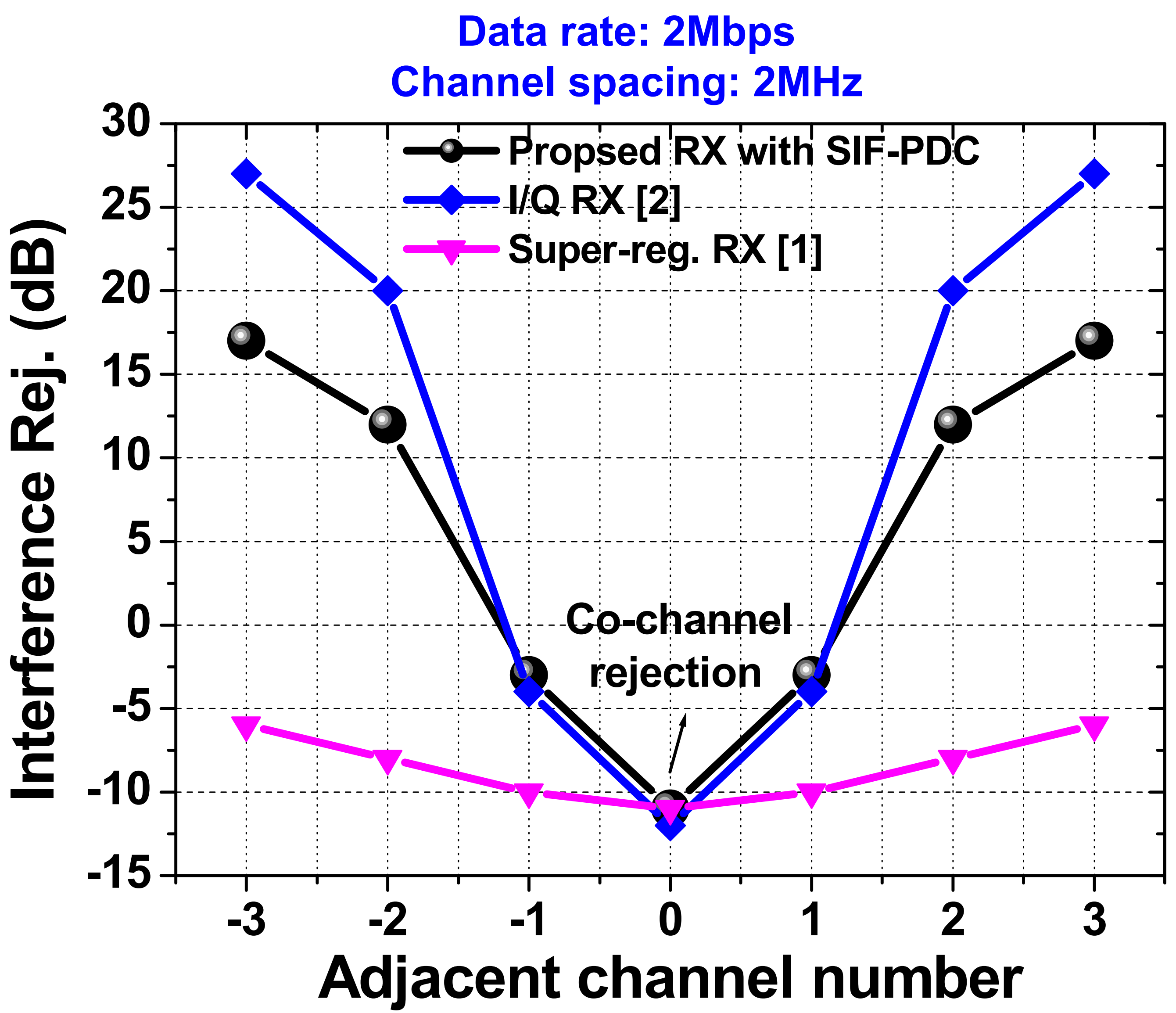
RX LPF and comparator output (f_{OUT})



Phase integrator output (Φ_{OUT})

- The RX demodulates frequency/phase, and directly provides digitized outputs

RX Selectivity



Comparison Table

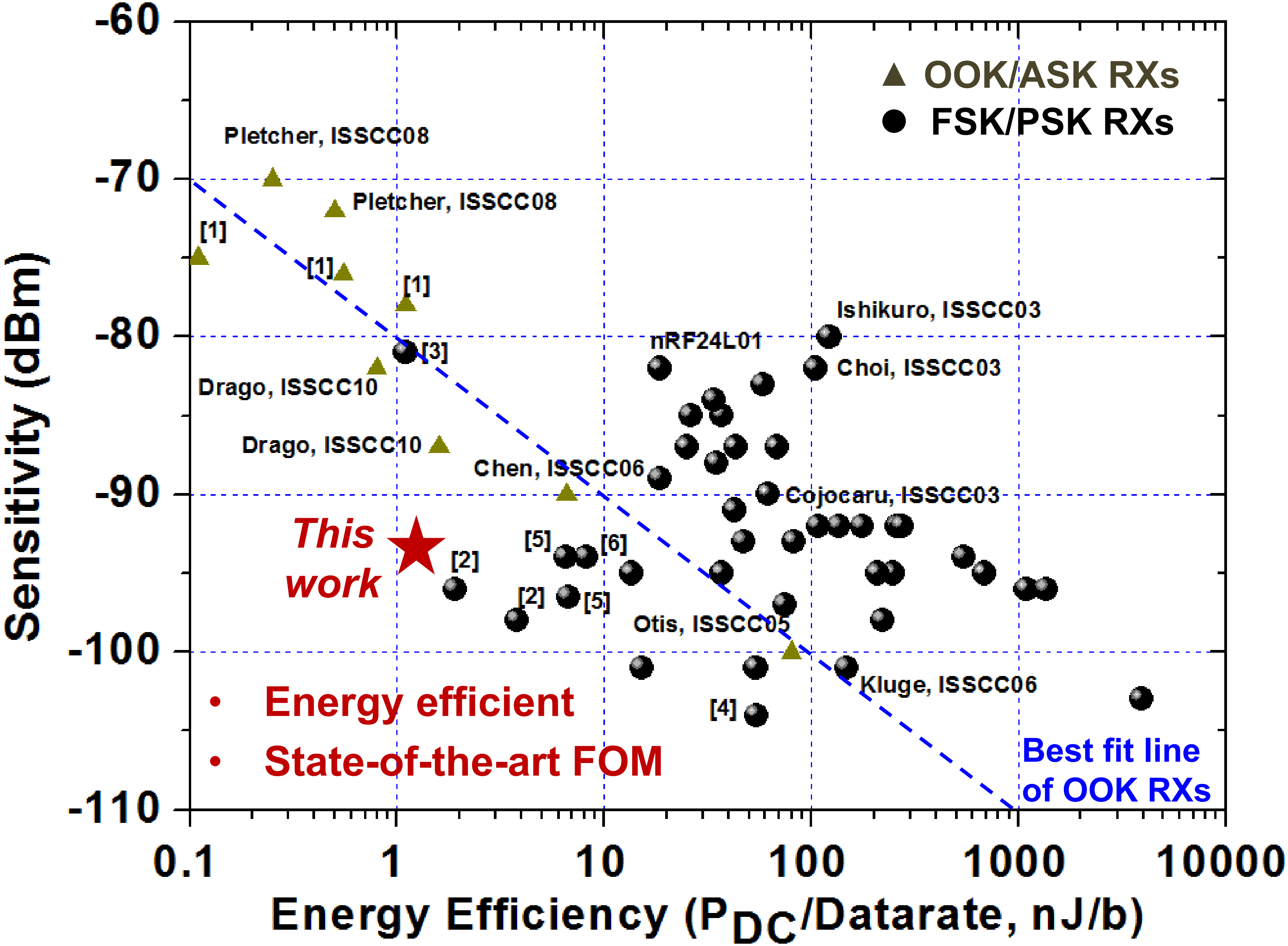
	This work	[1]	[2]	[3]	[5]	[6]
	ISSCC'14	ISSCC'11	ISSCC'13	MTT'13	ISSCC'12	VLSI'13
Data rate & modulation	2-Mbps HS-OQPSK	5-Mbps OOK	2-Mbps HS-OQPSK	1-Mbps GFSK	1-Mbps GFSK	1-Mbps GFSK
Technology	90nm	90nm	90nm	130nm	130nm	65nm
Architecture	SIF-PDC	Super reg.	Sliding-IF	Phase ADC	Sliding-IF	Zero-IF
Supply voltage	1 V	1/1.2V	1.2 V	1V	1/1.5 V	1.3V
Power cons.	2.4mW	0.53mW	3.8mW	1.1mW	6.5mW	8.2mW
Sensitivity*	-92dBm	-75dBm	-96dBm	-81dBm	-94dBm	-94dBm
ACR ($2^{nd}/3^{rd}$)**	**12/17dB**	-8/-6dB	20/27dB	N.A.	N.A.	N.A.
RX energy eff.	**1.2nJ/b**	0.1nJ/b	1.9nJ/b	1.1nJ/b	6.5nJ/b	8.2nJ/b
FOM***	181	175	183	171	175	174

* Based on BER of 10^{-3} without error corrections

** ETSI EN 300 440-1 V1.3.1 (2001-09) page 27

*** RX FOM = - Sensitivity -10*log(P_{DC} / Data rate)

2.4GHz ULP RX Benchmark



Conclusion

- A novel phase-tracking RX architecture based on multi-phase selection is proposed for low-power applications
  - 40% better energy efficiency
  - 25% smaller area
  - Sensitivity and selectivity are still comparable to conventional Cartesian I/Q RXs

- The proposed RX transforms the RF signal processing from the analog-amplitude to digital-phase domain
  - Less restricted by the supply voltage
  - Suitable for technology scaling

A 1.3mW 0.6V WBAN-Compatible Sub-Sampling PSK Receiver in 65nm CMOS

Jiao Cheng[1], Nan Qi[1], Patrick Yin Chiang[1,2], Arun Natarajan[1]

[1]Oregon State University, Corvallis, OR

[2]Fudan University, Shanghai, China

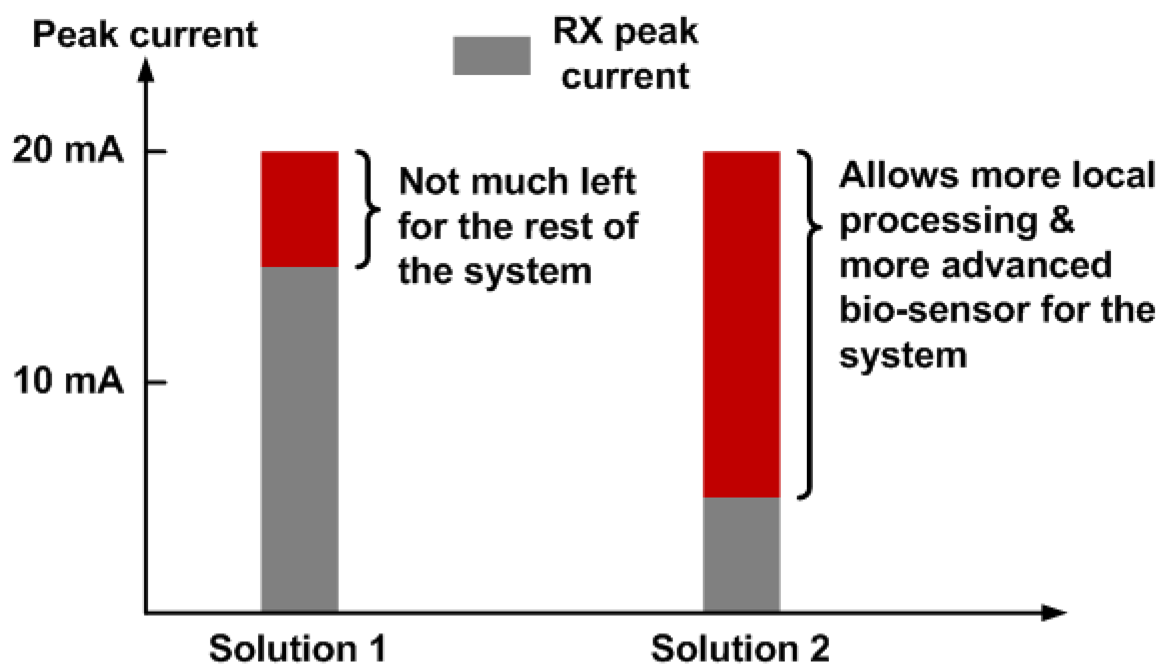
Outline

- Challenges in low-power wireless receiver design
- Feasibility of proposed sub-sampling architecture
- Design of building blocks
- Measurement results
- Conclusion

Application and Design Target

- 802.15.6 (WBAN) is a wireless standard targeted at replacing cables in biomedical applications
  - ➢ Lower power consumption improves battery’s size, cost, lifetime
  - ➢ Lower peak current allows more system flexibility

CR2032 can deliver ~20mA peak

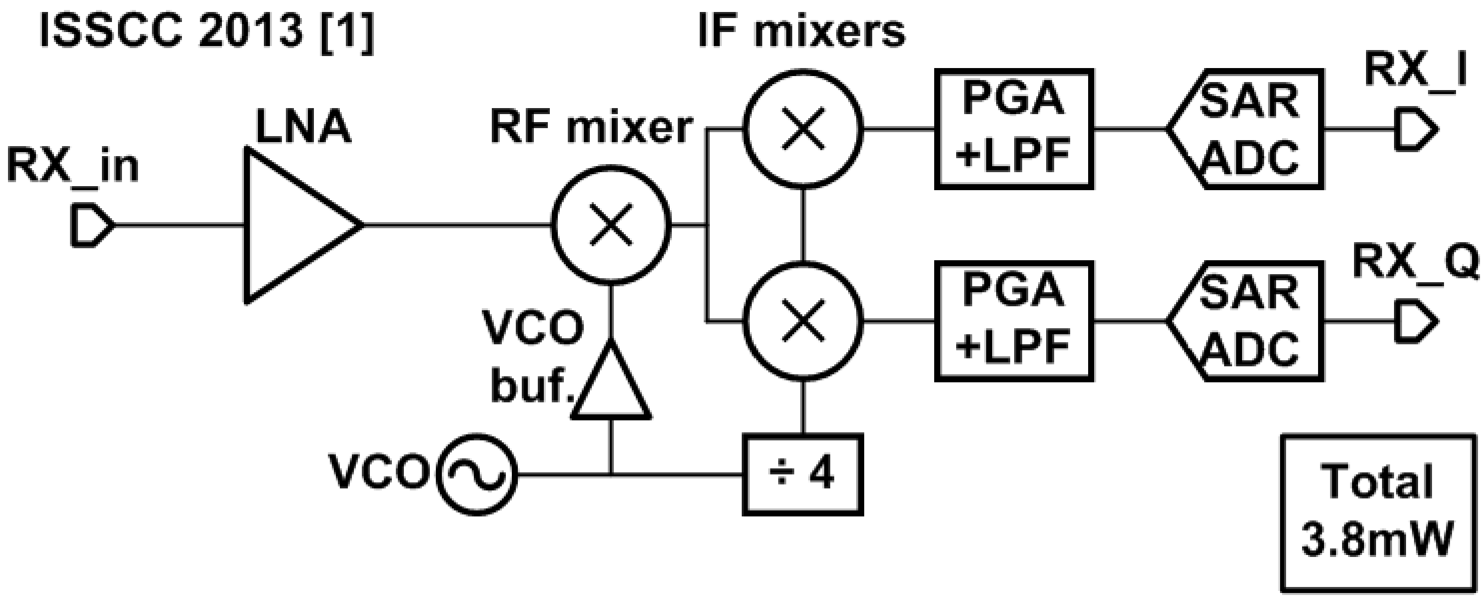


- Design targets ~1mW average power with ~2mA peak current

Challenges

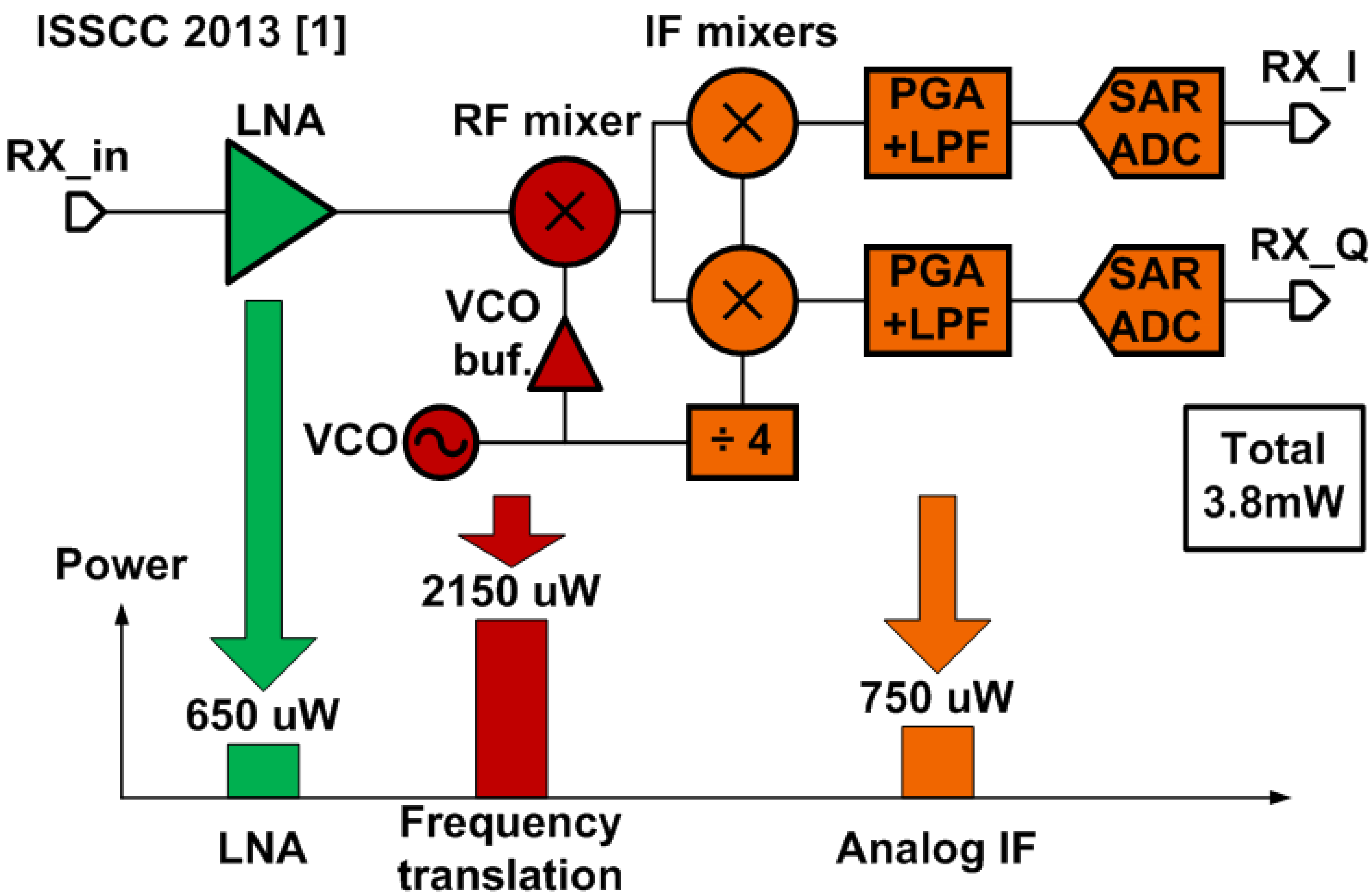
- High frequency LO
- Analog IF

Challenges in Low Power Design [1]



[1] Yao-Hong Liu et al., *ISSCC Dig. Tech Papers*, pp. 446-447, Feb. 2013.

Challenges in Low Power Design [1]



[1] Yao-Hong Liu et al., *ISSCC Dig. Tech Papers*, pp. 446-447, Feb. 2013.

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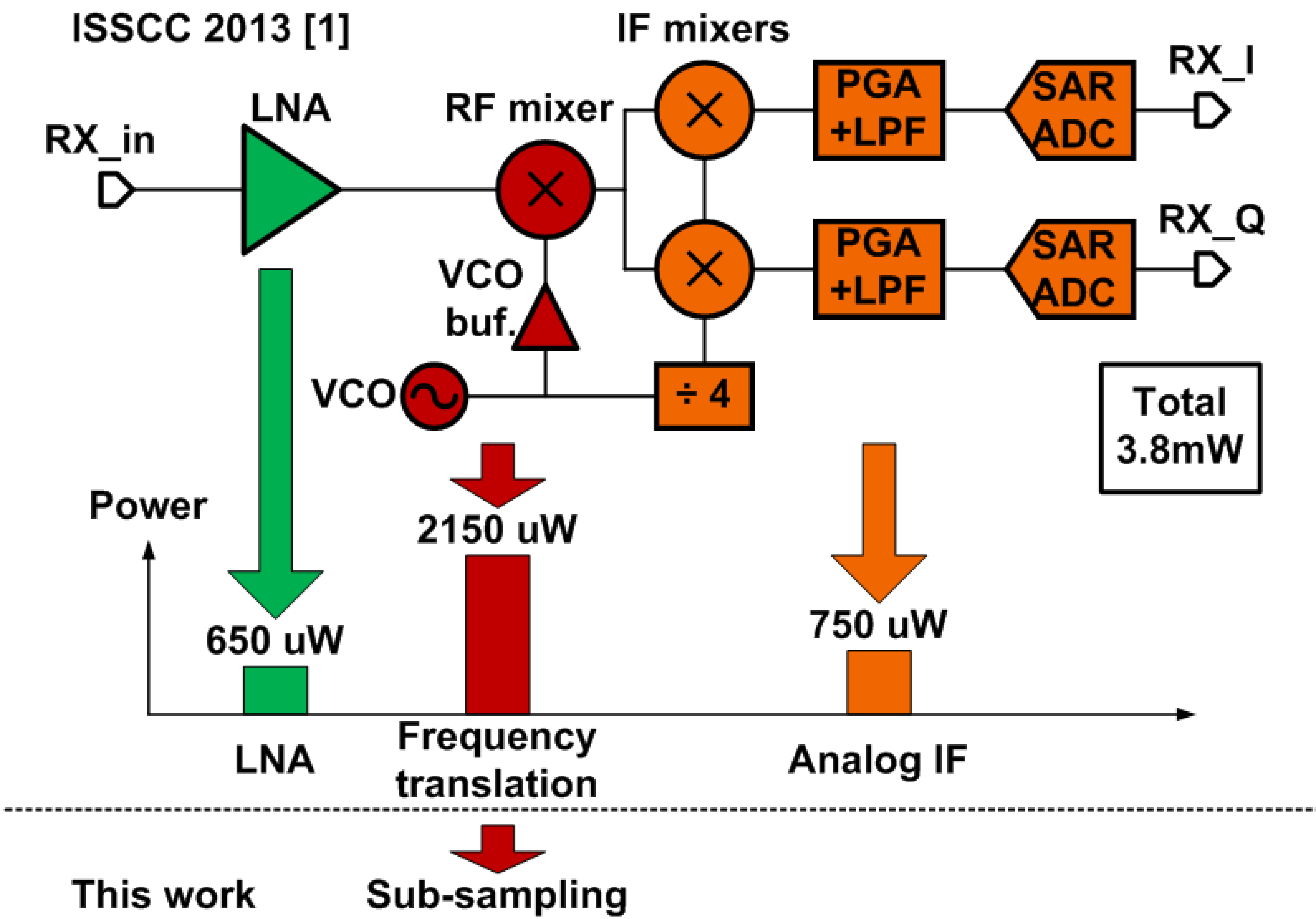
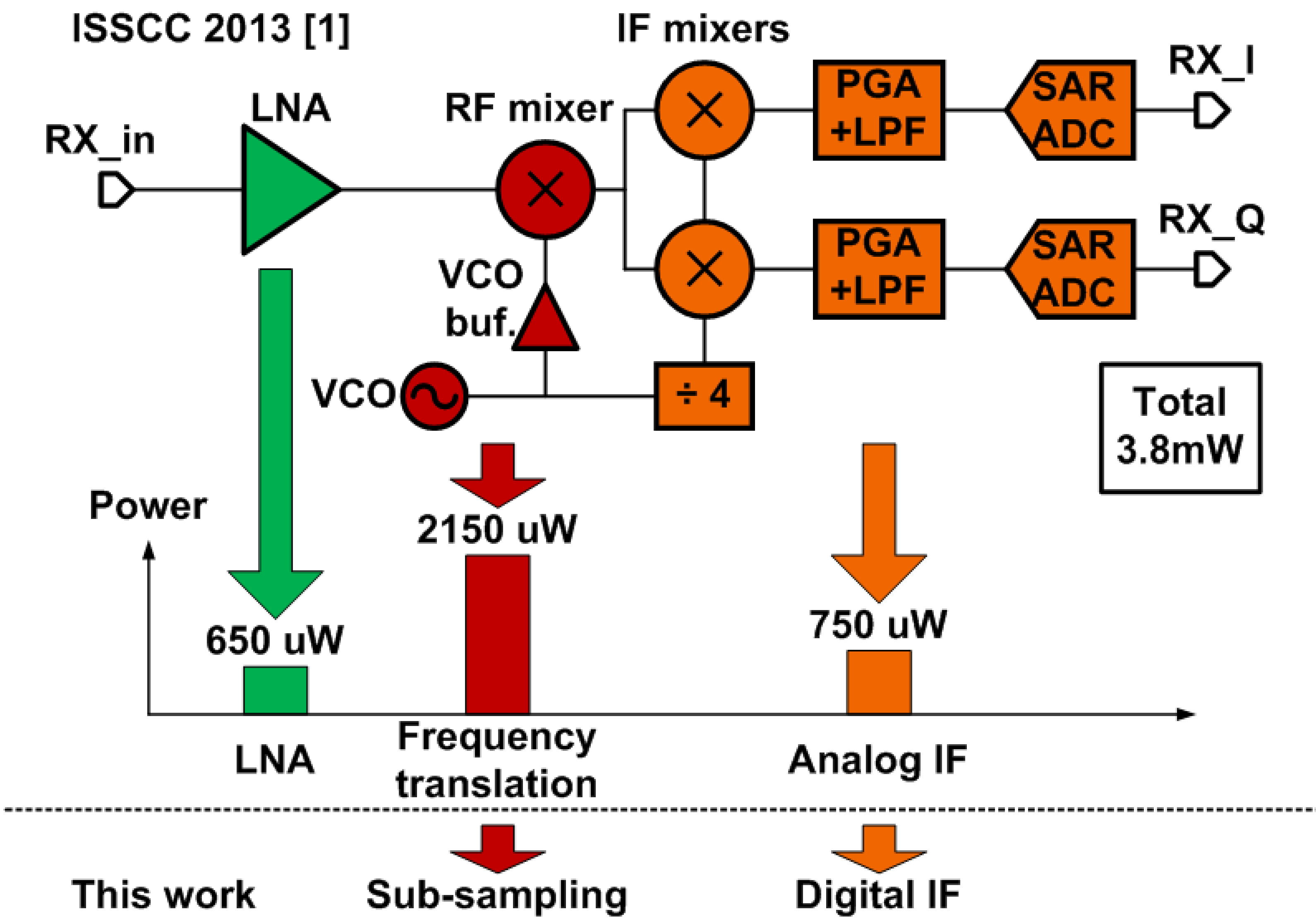


[1] Yao-Hong Liu et al., *ISSCC Dig. Tech Papers*, pp. 446-447, Feb. 2013.

Challenges in Low Power Design [1]

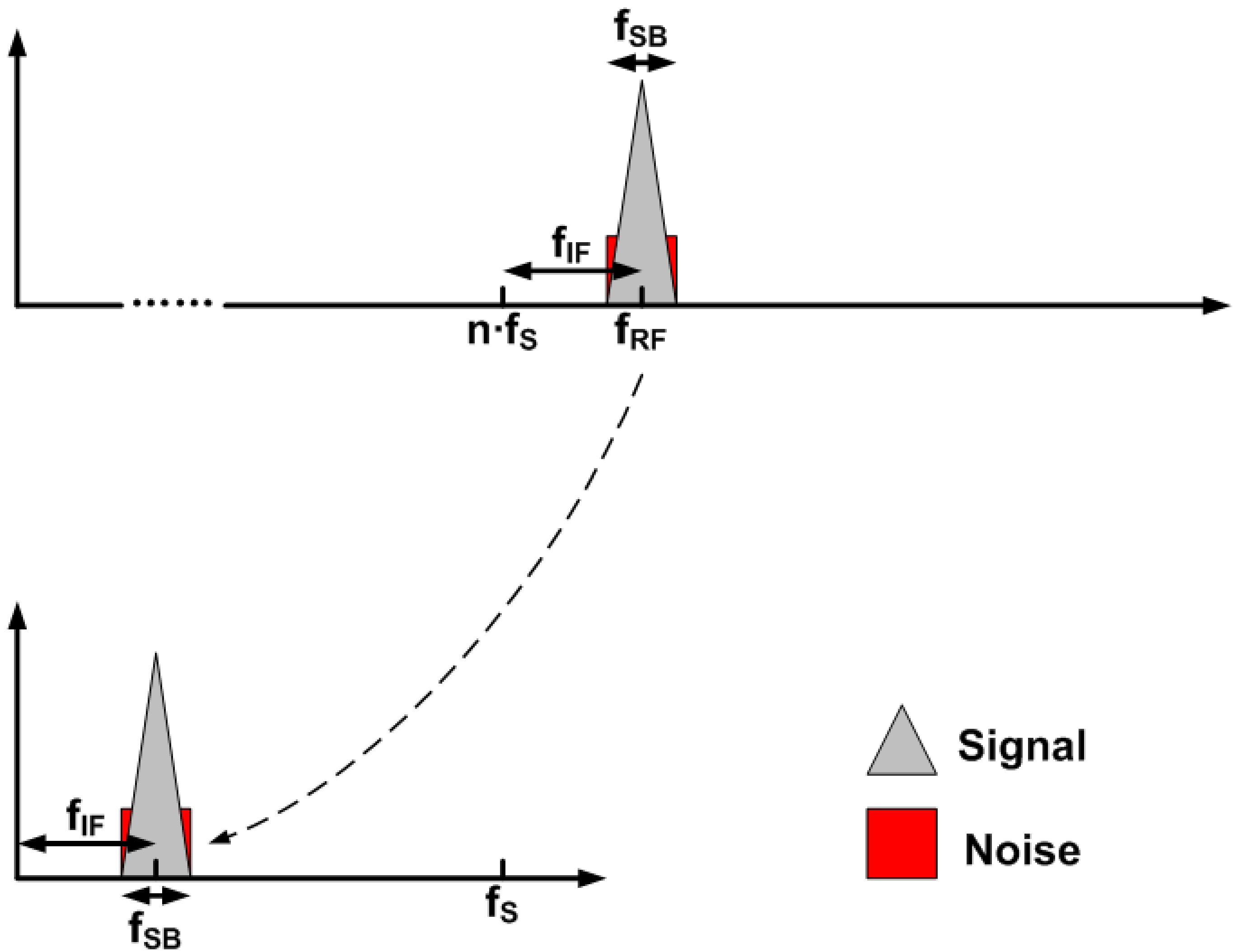


[1] Yao-Hong Liu et al., *ISSCC Dig. Tech Papers*, pp. 446-447, Feb. 2013.

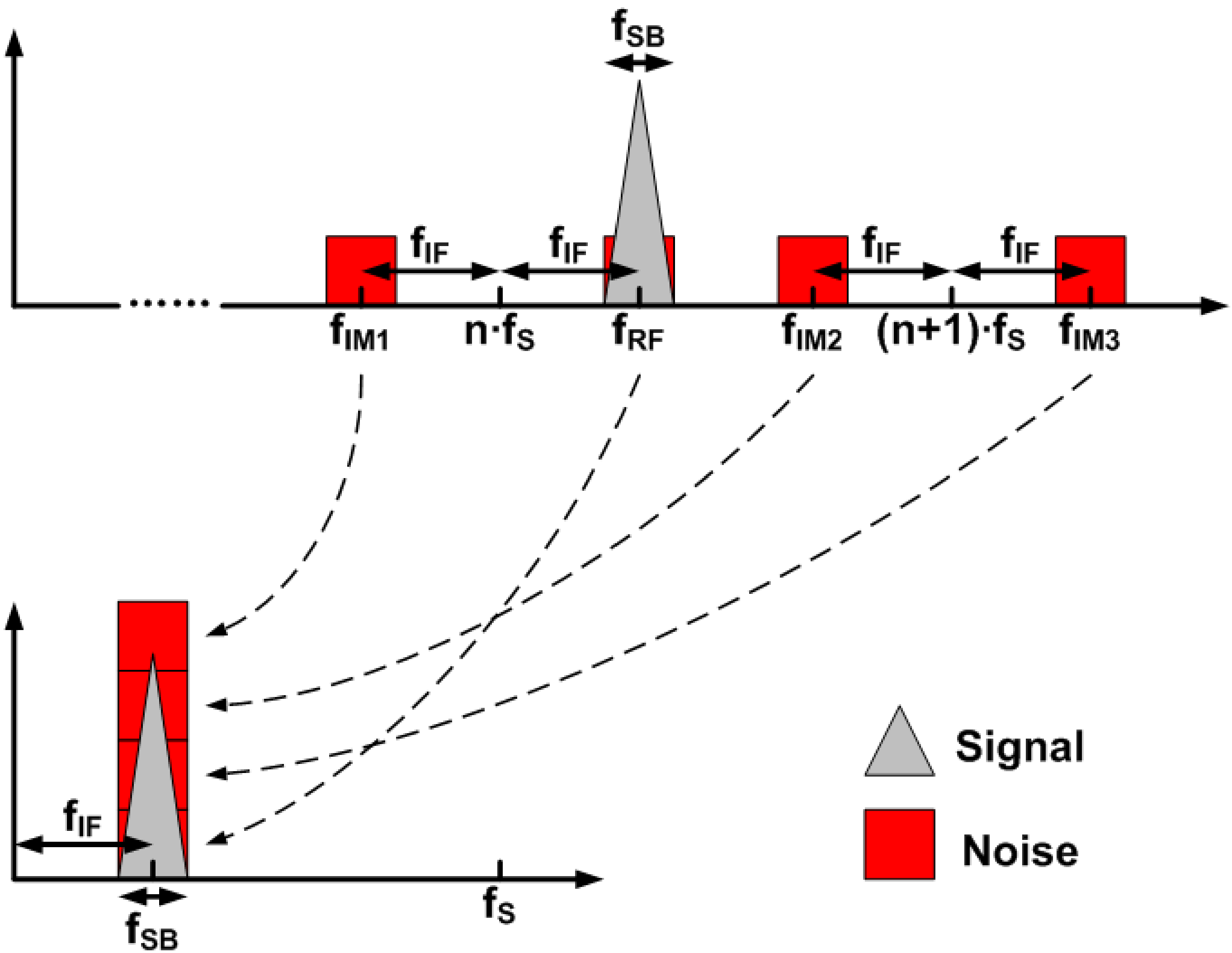
Feasibility

- Noise folding suppression
- Gain augmentation

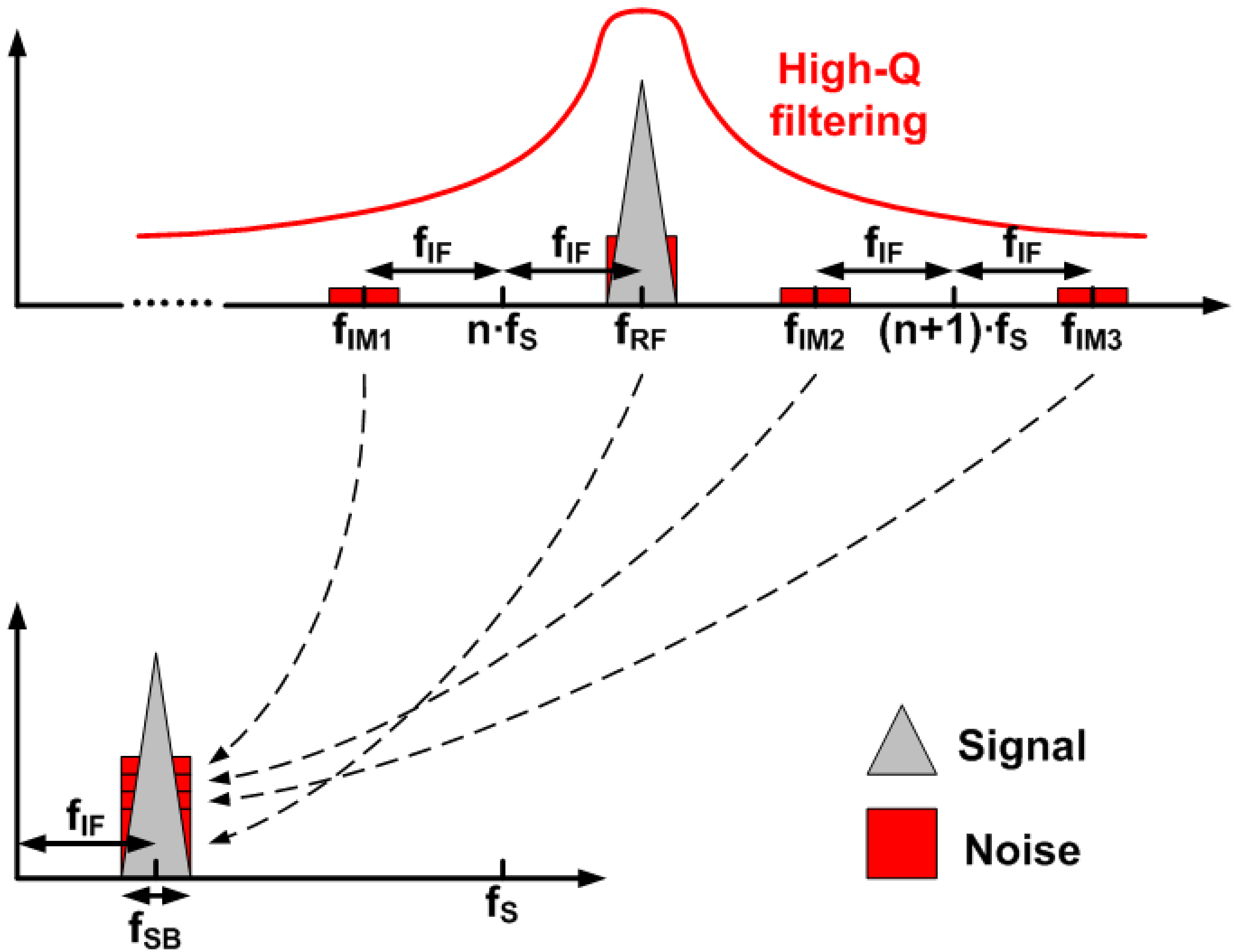
Sub-Sampling Principle



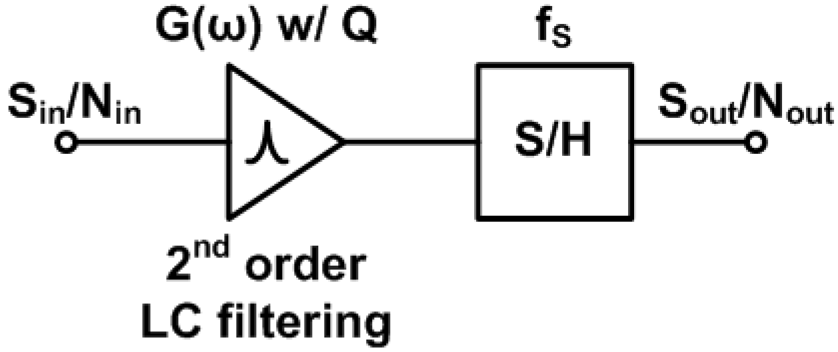
Noise folding in Sub-Sampling RX



High-Q filtering to Mitigate Noise Folding



Criteria for Low NF Operation



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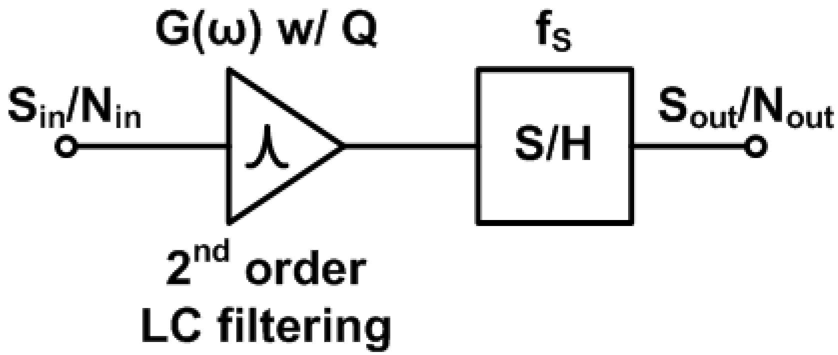
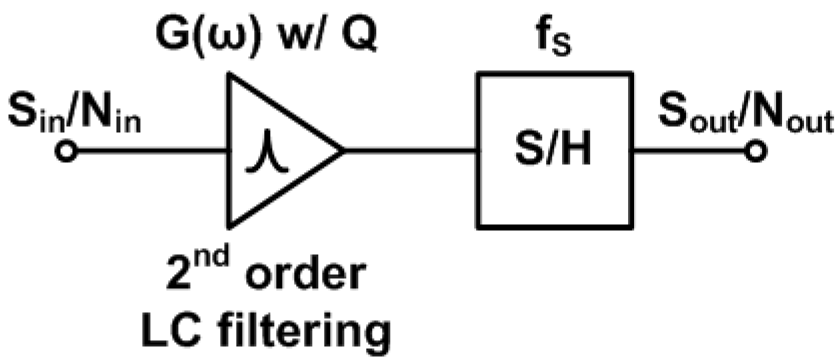


$$F_{overall} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}}$$

$$= F_{G(\omega_0)} \sum_{k=0}^{\infty} \frac{G\left(\omega_0 \pm k\frac{\omega_s}{2}\right)}{G(\omega_0)}$$

Criteria for Low NF Operation



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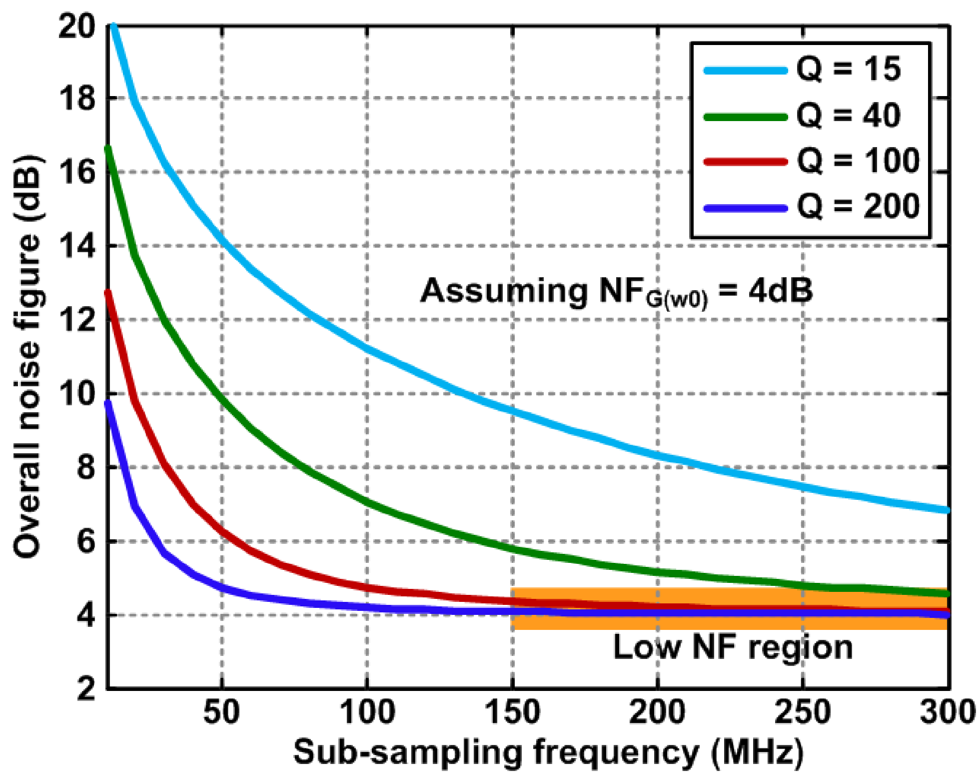
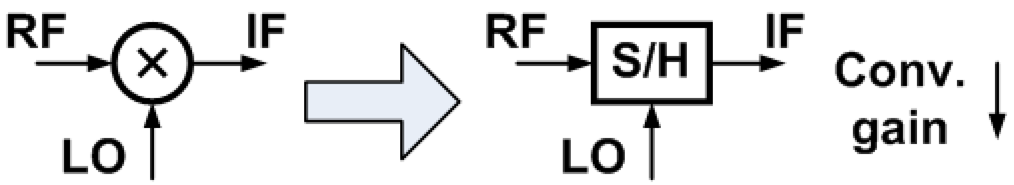


Low NF criteria @ 2.4GHz carrier

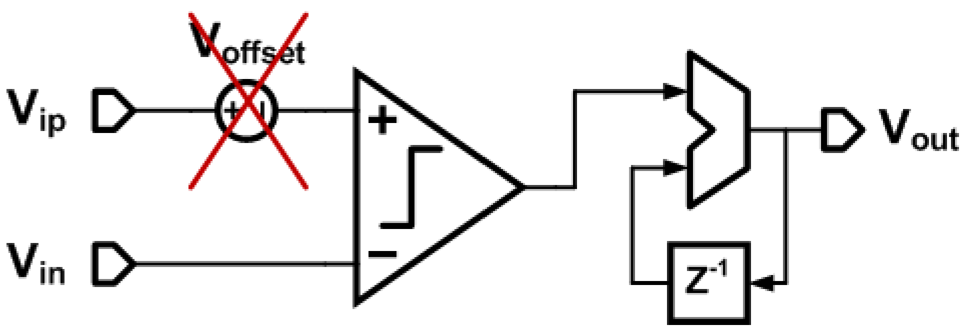
- **filter Q > 100**
- **sampling f_S > 150 MHz**

Gain Augmentation in Sub-Sampling Receiver

- Passive sub-sampler reduces conversion gain (CG)



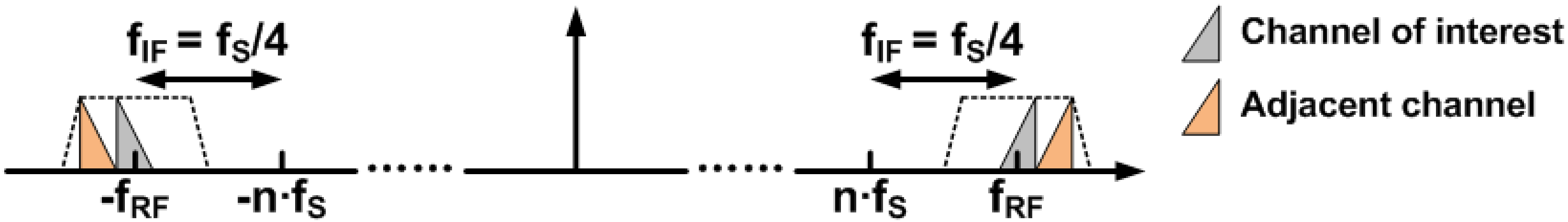
- The reduction in CG is compensated by increasing both RF and IF gain
  - ➢ RF: Q-enhancement LNA → higher gain
  - ➢ IF: 1-b A-D quantizer → "infinite" gain after DC offset calibration



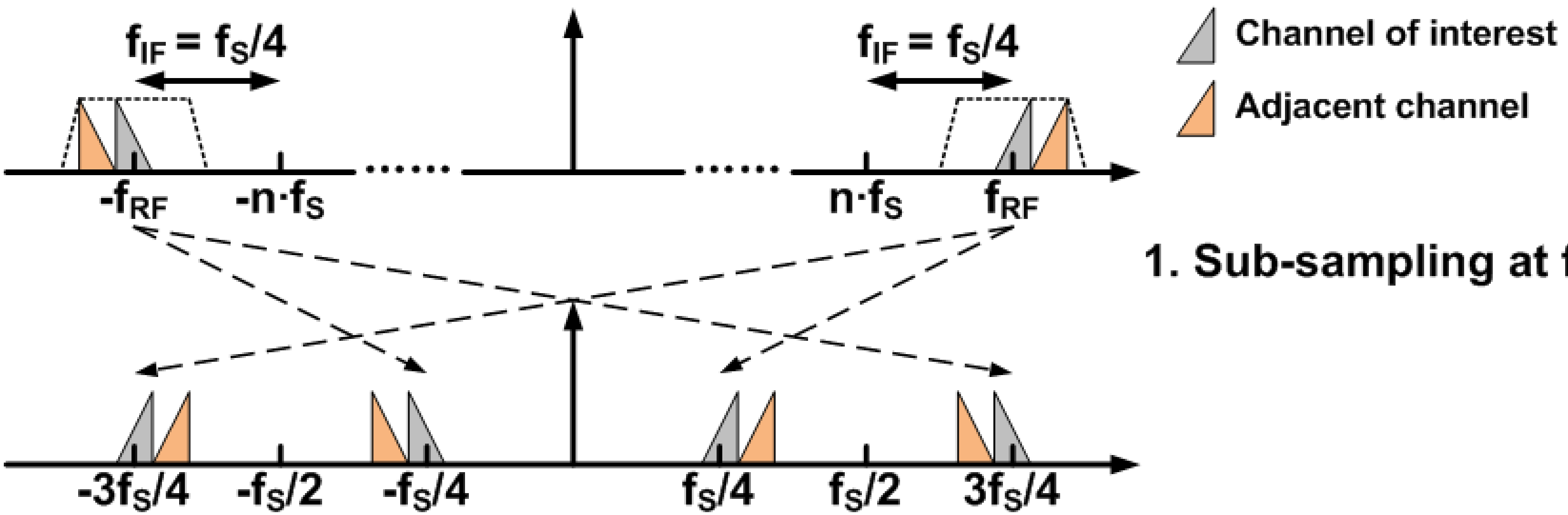
Circuit Design

- Sub-sampling architecture
- Digital-intensive design

Top-Level | Frequency Plan

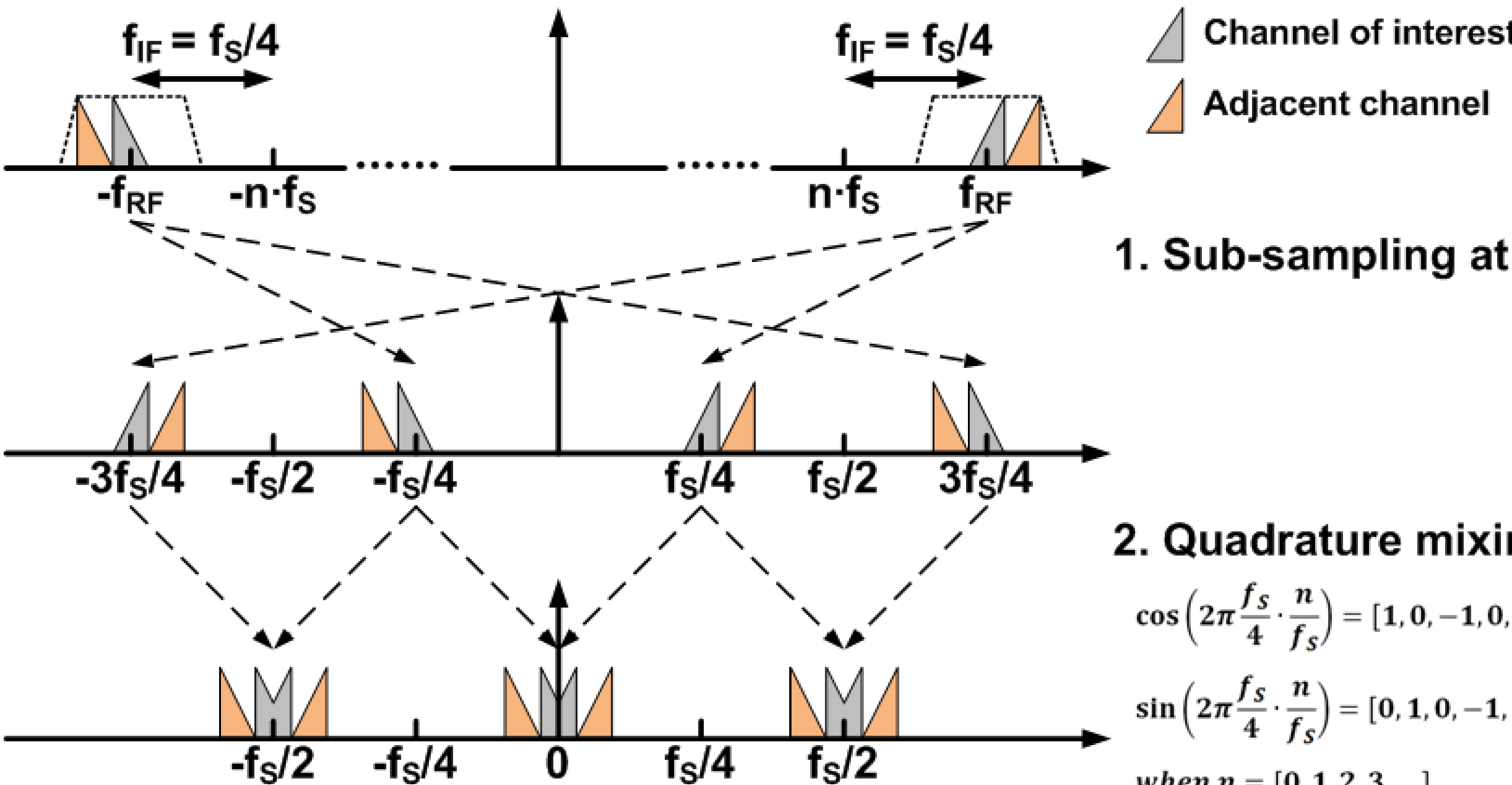


Top-Level | Frequency Plan



1. Sub-sampling at f_S

Top-Level | Frequency Plan



1. Sub-sampling at f_S

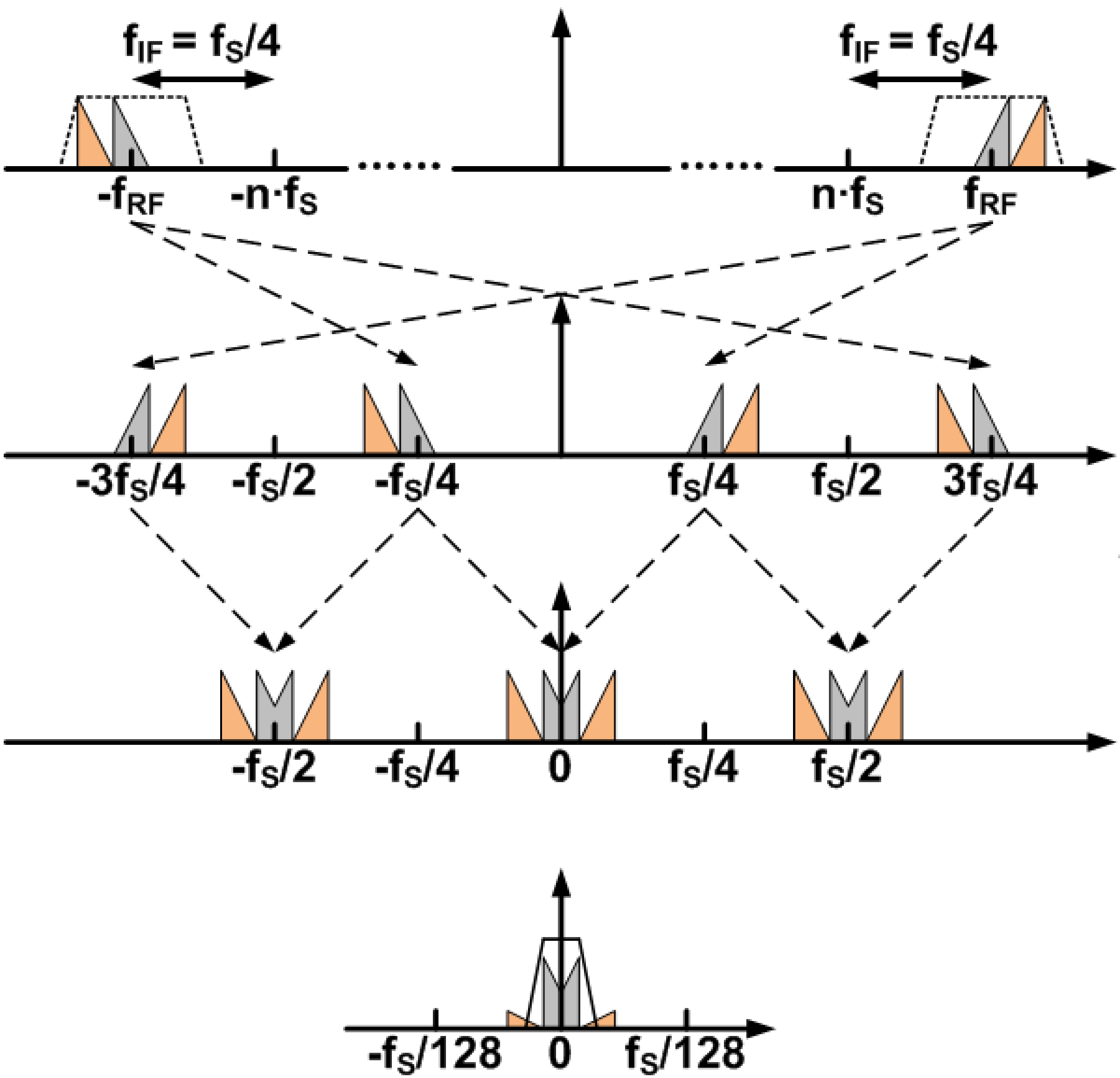
2. Quadrature mixing

$$\cos\left(2\pi \frac{f_S}{4} \cdot \frac{n}{f_S}\right) = [1, 0, -1, 0, \dots]$$

$$\sin\left(2\pi \frac{f_S}{4} \cdot \frac{n}{f_S}\right) = [0, 1, 0, -1, \dots]$$

$$when\ n = [0, 1, 2, 3, \dots]$$

Top-Level | Frequency Plan



Channel of interest

Adjacent channel

1. Sub-sampling at f_S

2. Quadrature mixing

$$\cos\left(2\pi \frac{f_S}{4} \cdot \frac{n}{f_S}\right) = [1, 0, -1, 0, \ldots]$$

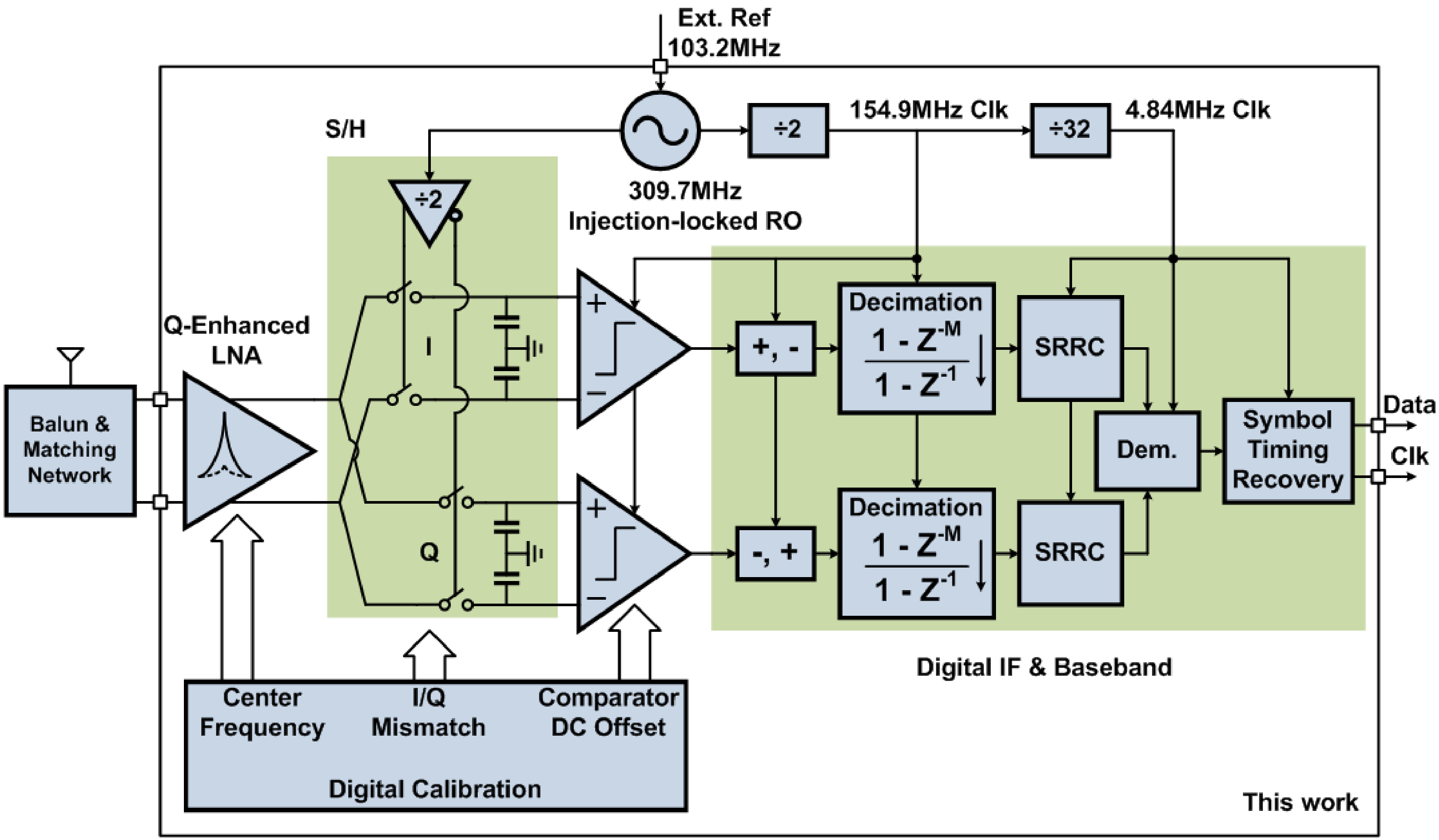
$$\sin\left(2\pi \frac{f_S}{4} \cdot \frac{n}{f_S}\right) = [0, 1, 0, -1, \ldots]$$

$$when\ n = [0, 1, 2, 3, \ldots]$$

3. Decimation filtering

Top-Level | System Block Diagram

- Sub-sampling mixing enables low frequency LO
- Digital IF stage reduces power consumption and die area



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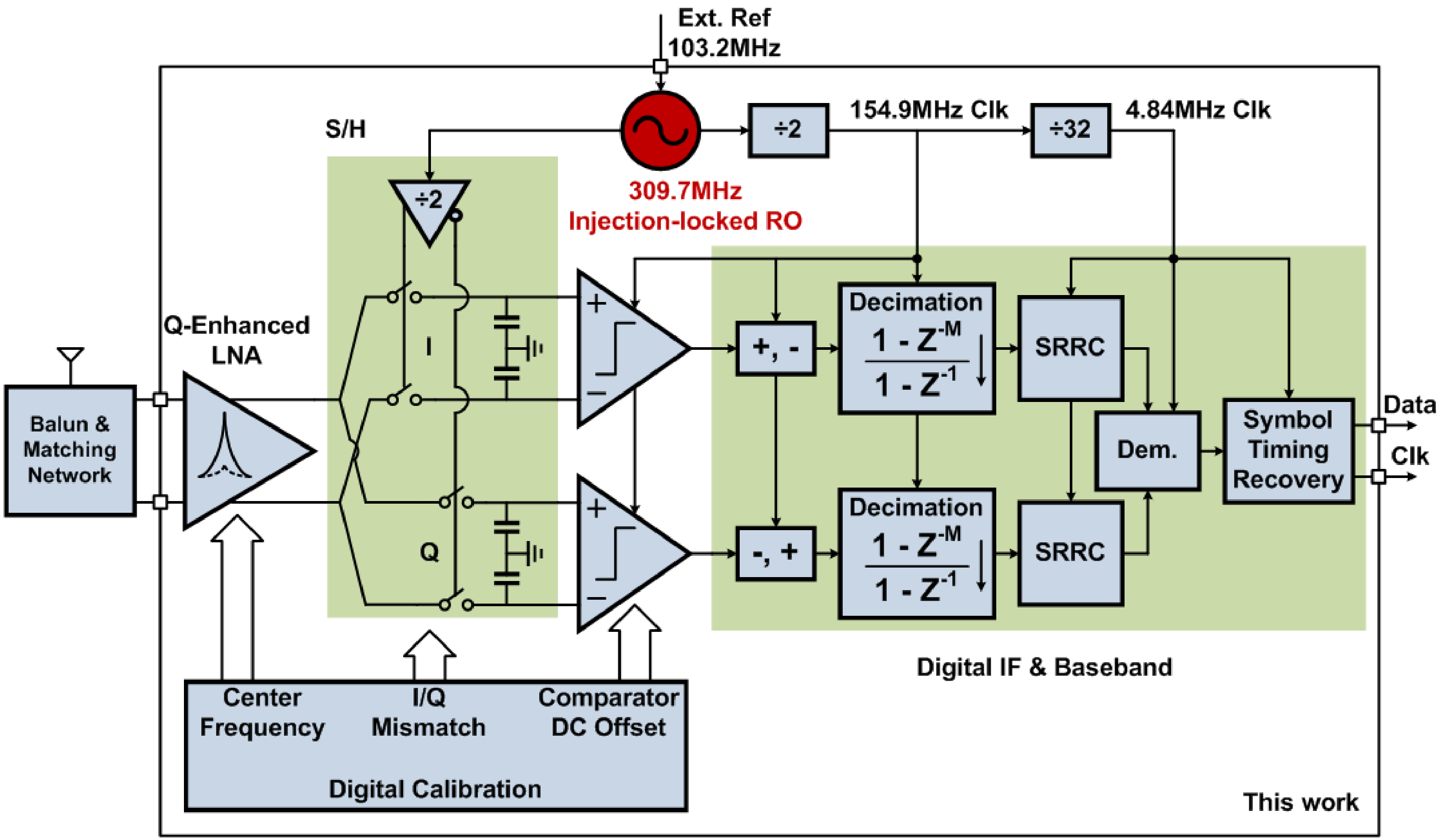

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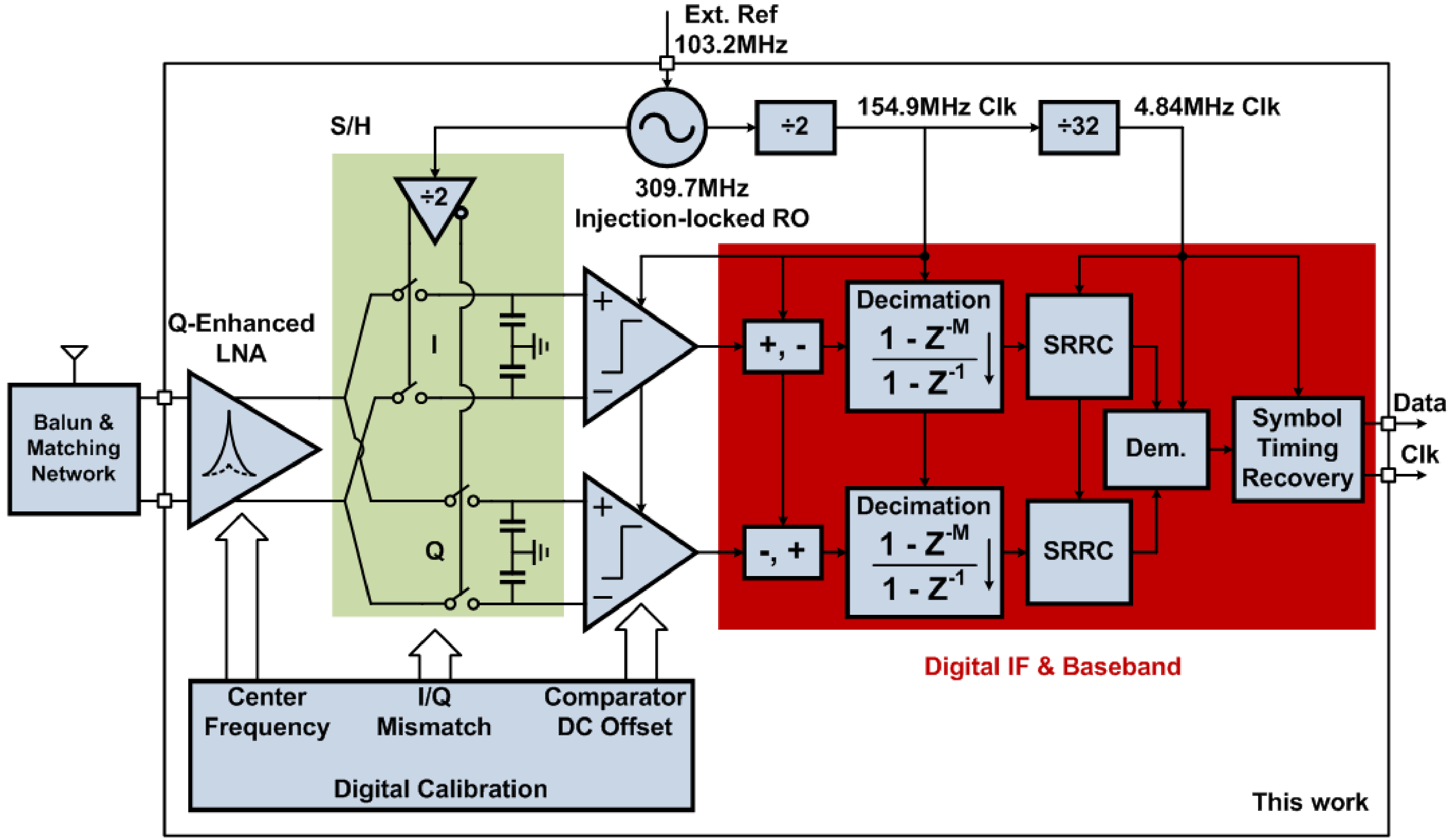

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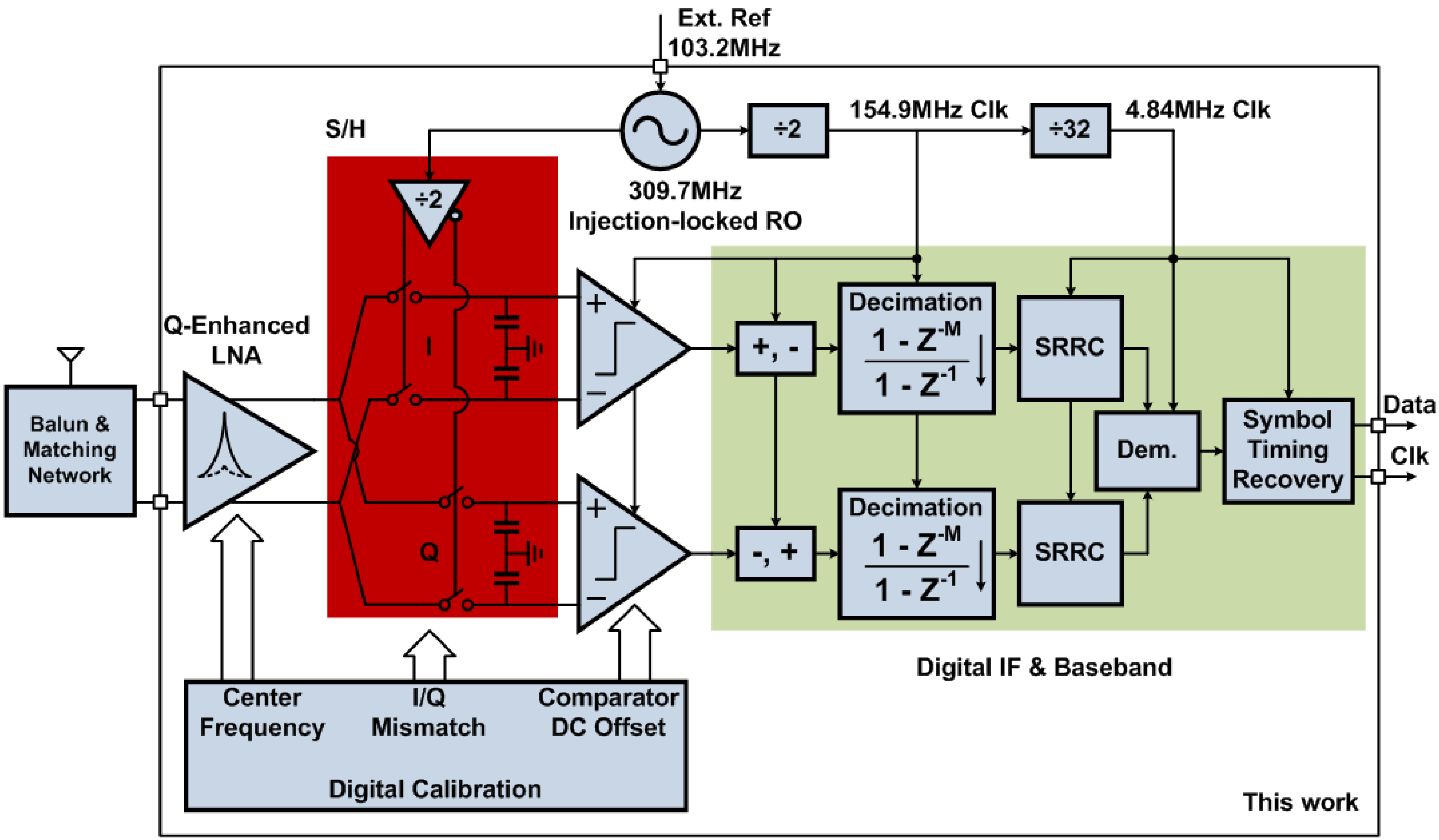
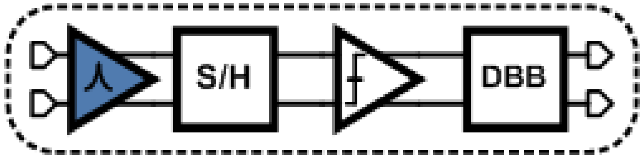
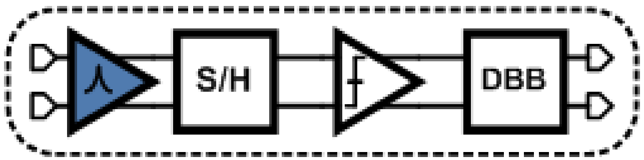


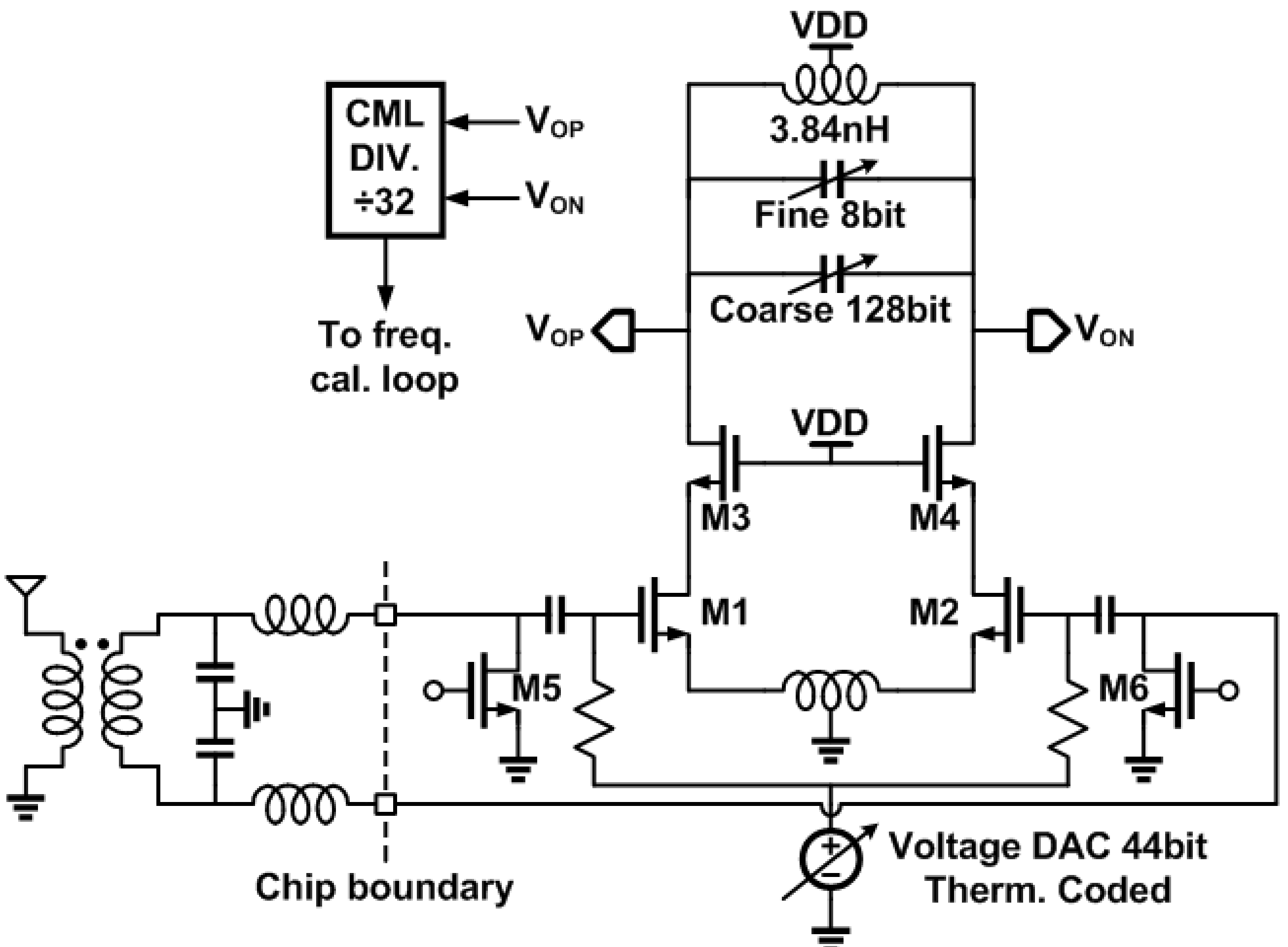
Circuits | Q-Enhancement in LNA



Circuits | Q-Enhancement in LNA

- Targeted filter Q is ~150
- Calibration facilitates high-Q operation





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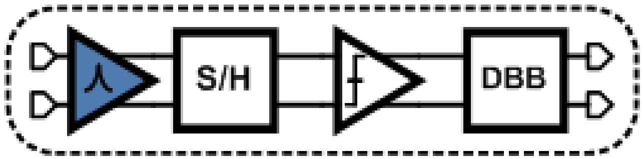

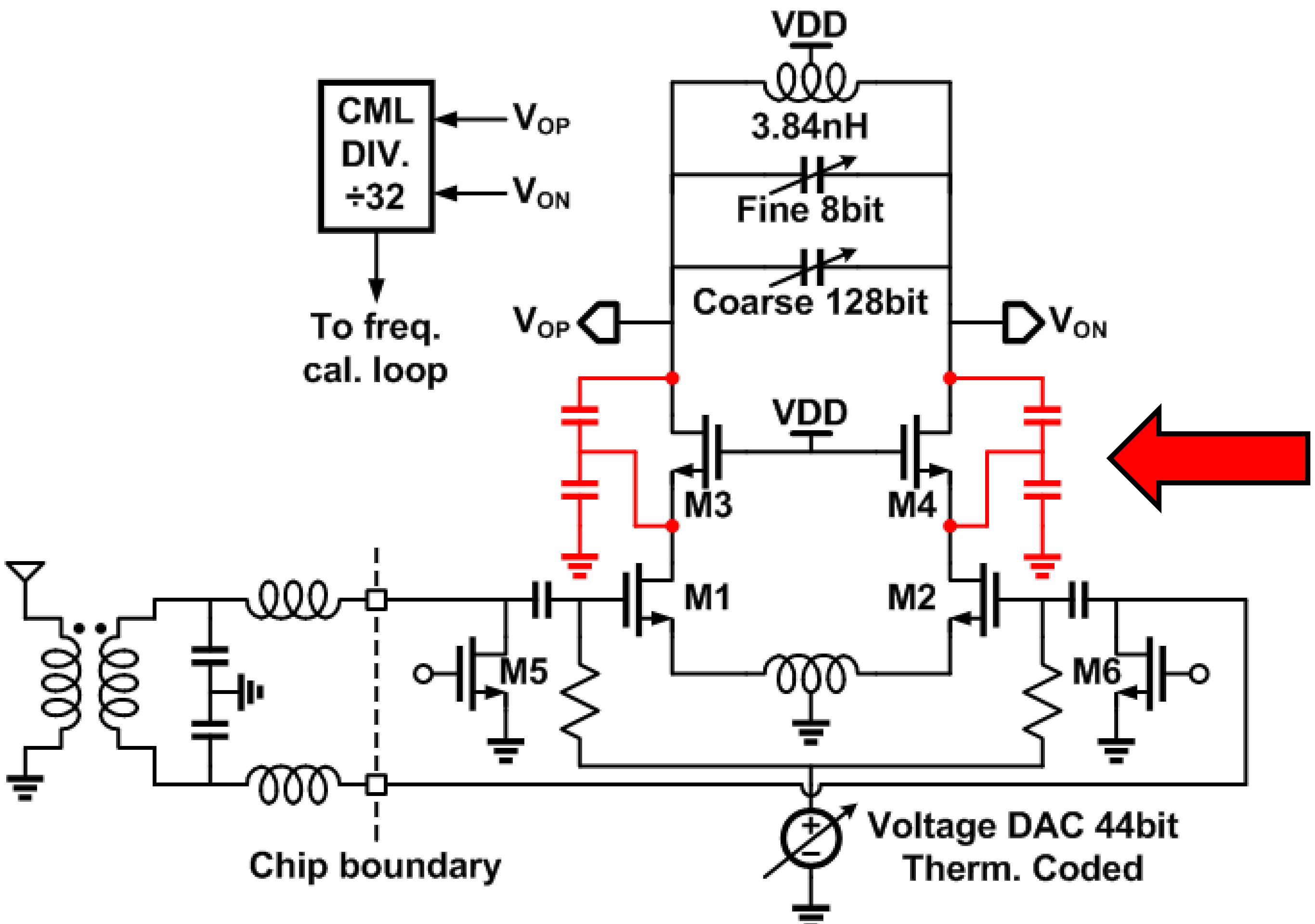

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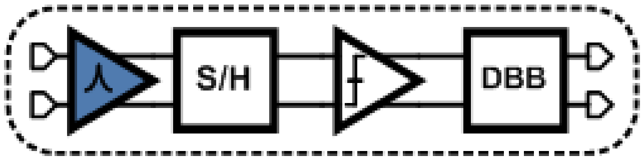

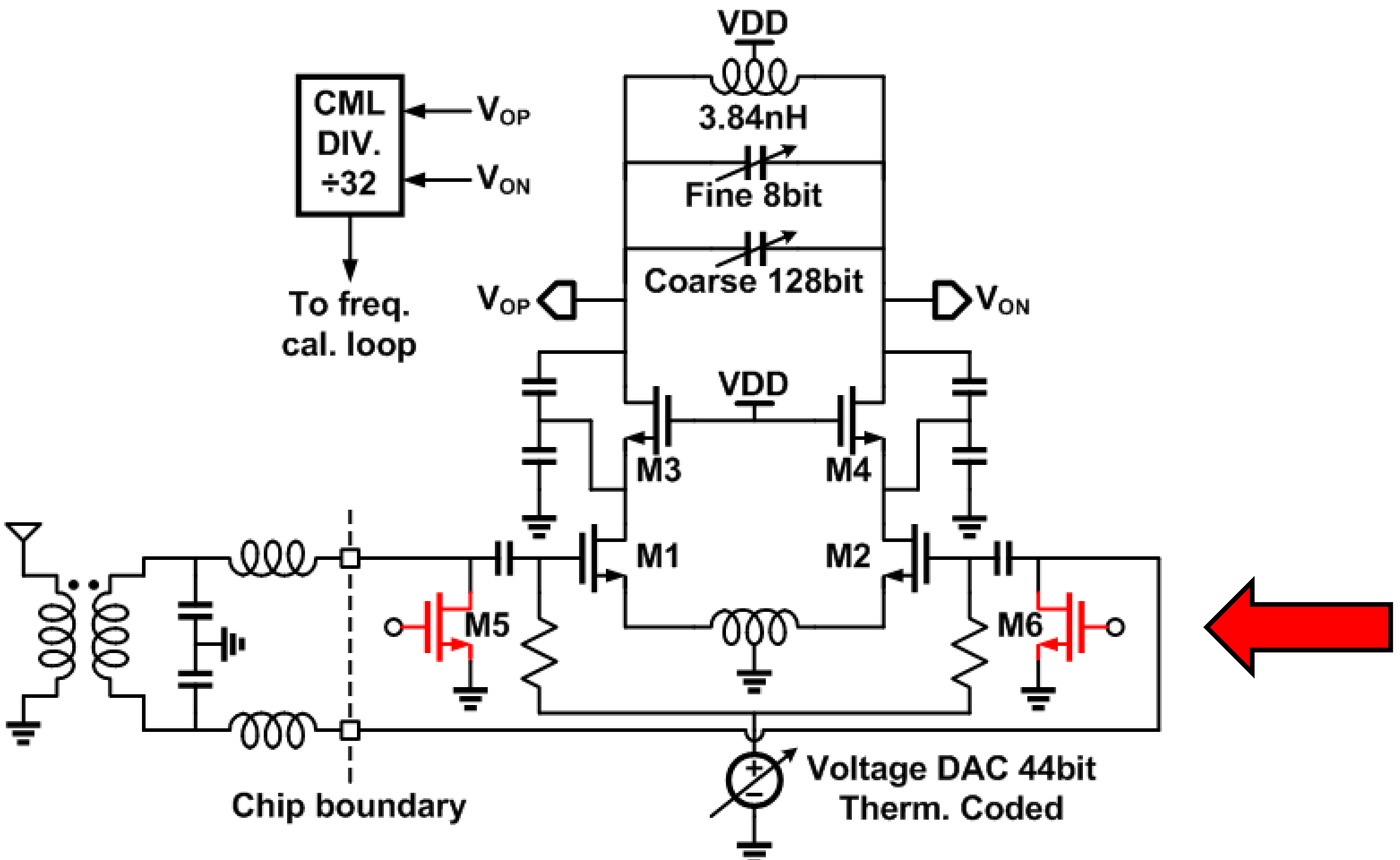

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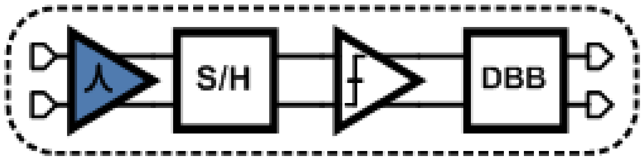
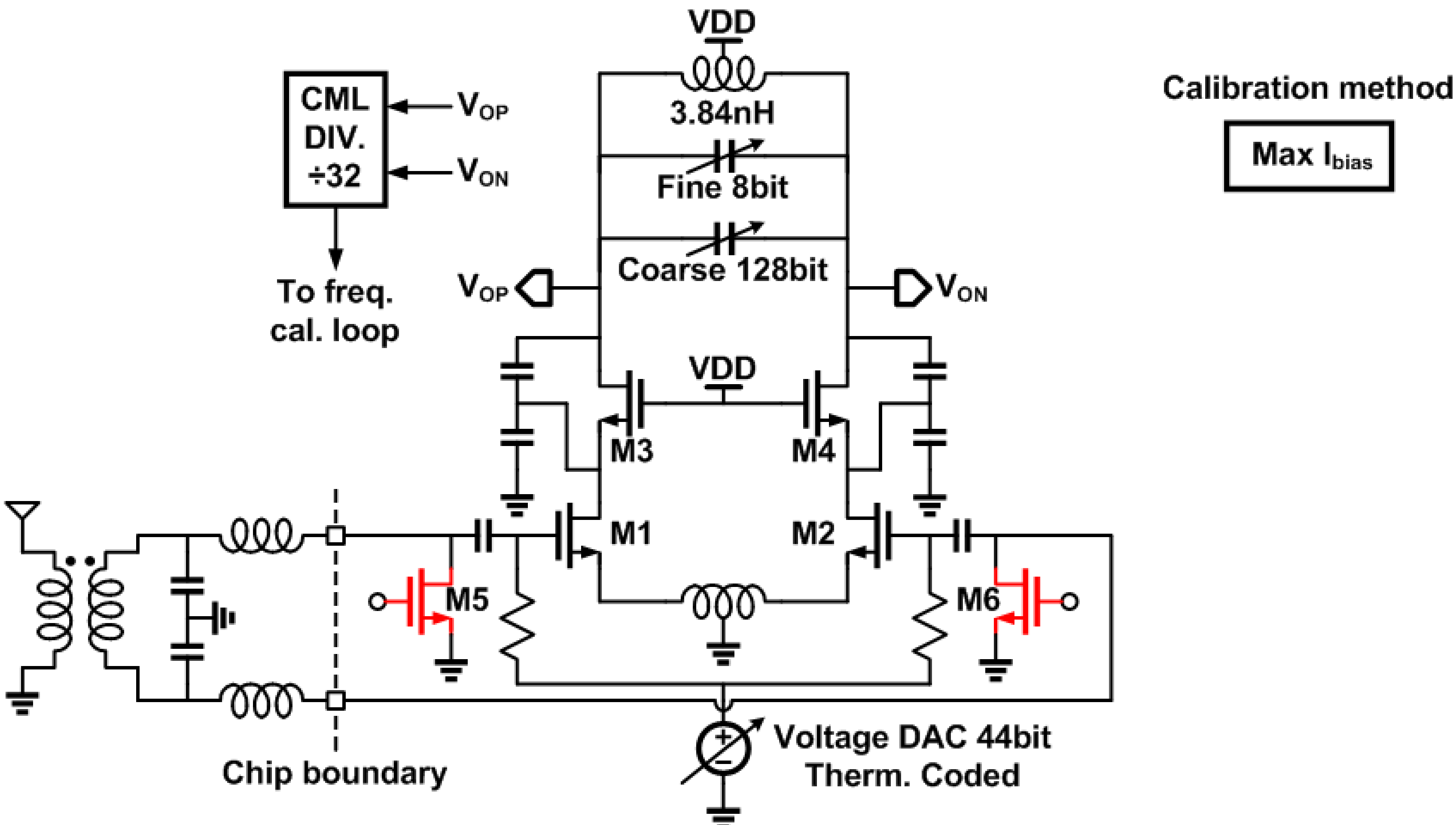
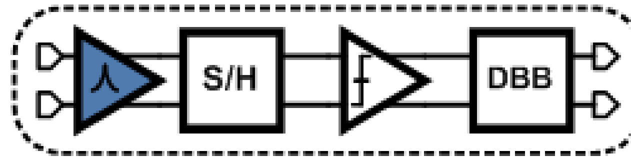
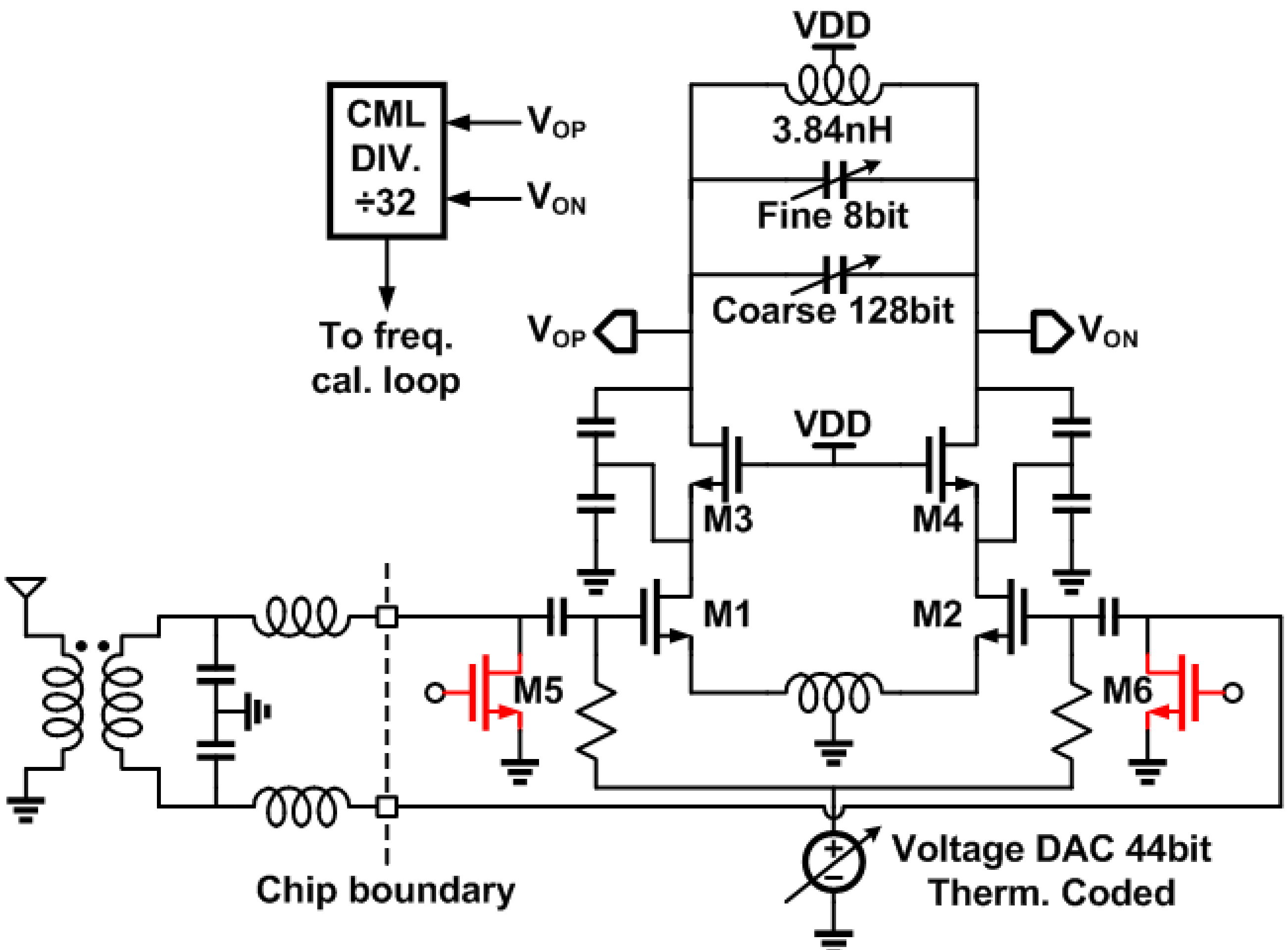




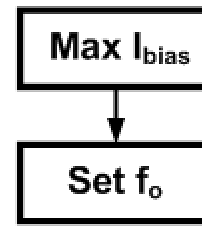
Circuits | Q-Enhancement in LNA

- Targeted filter Q is ~150
- Calibration facilitates high-Q operation





Calibration method



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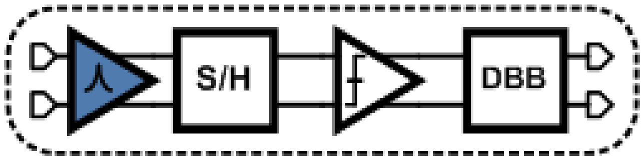

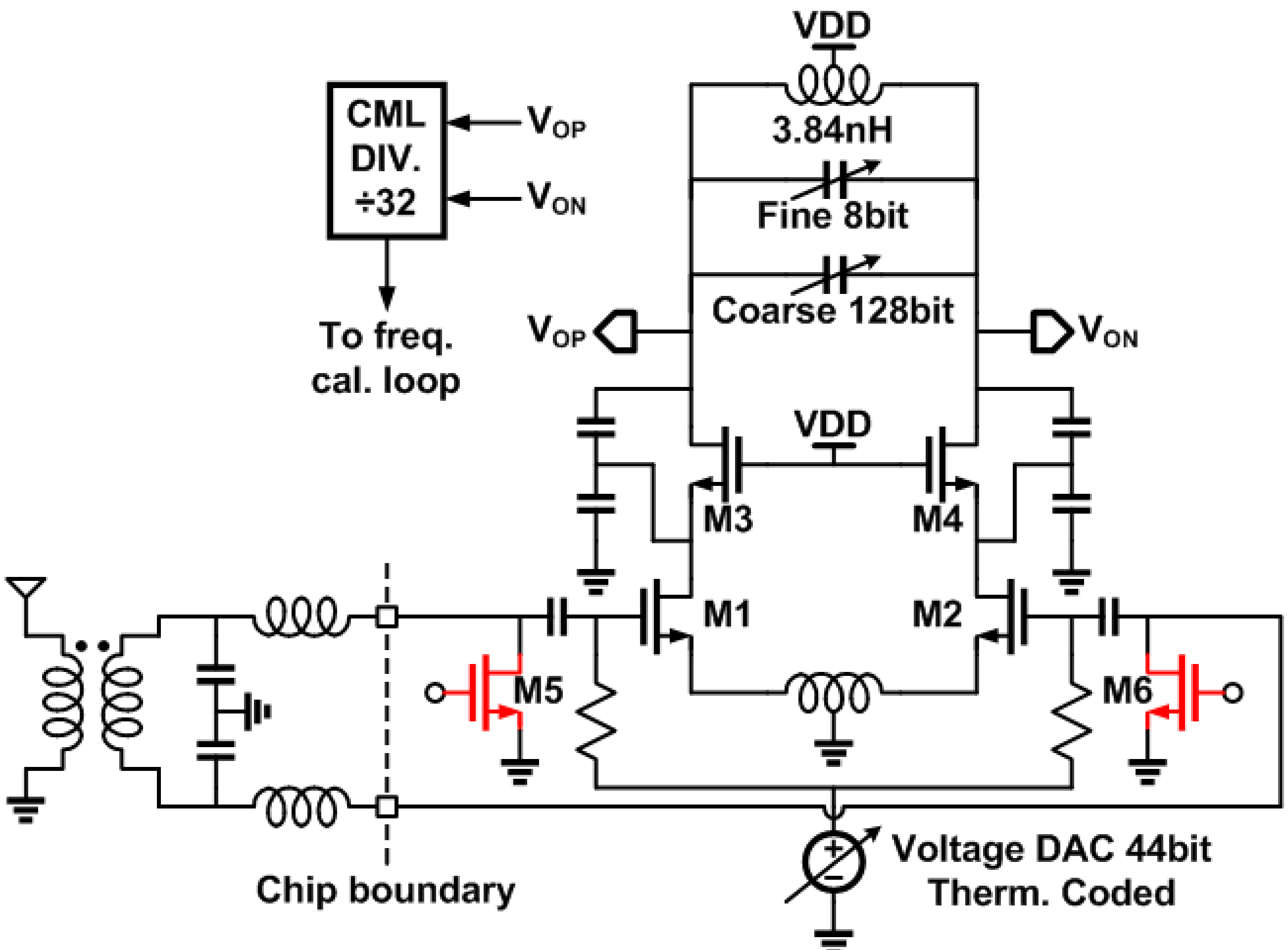

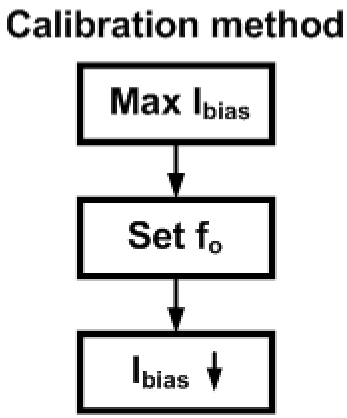

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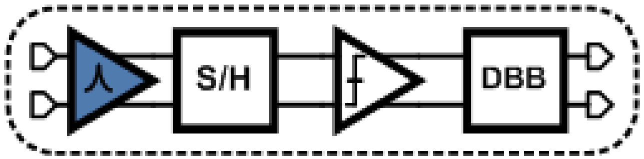
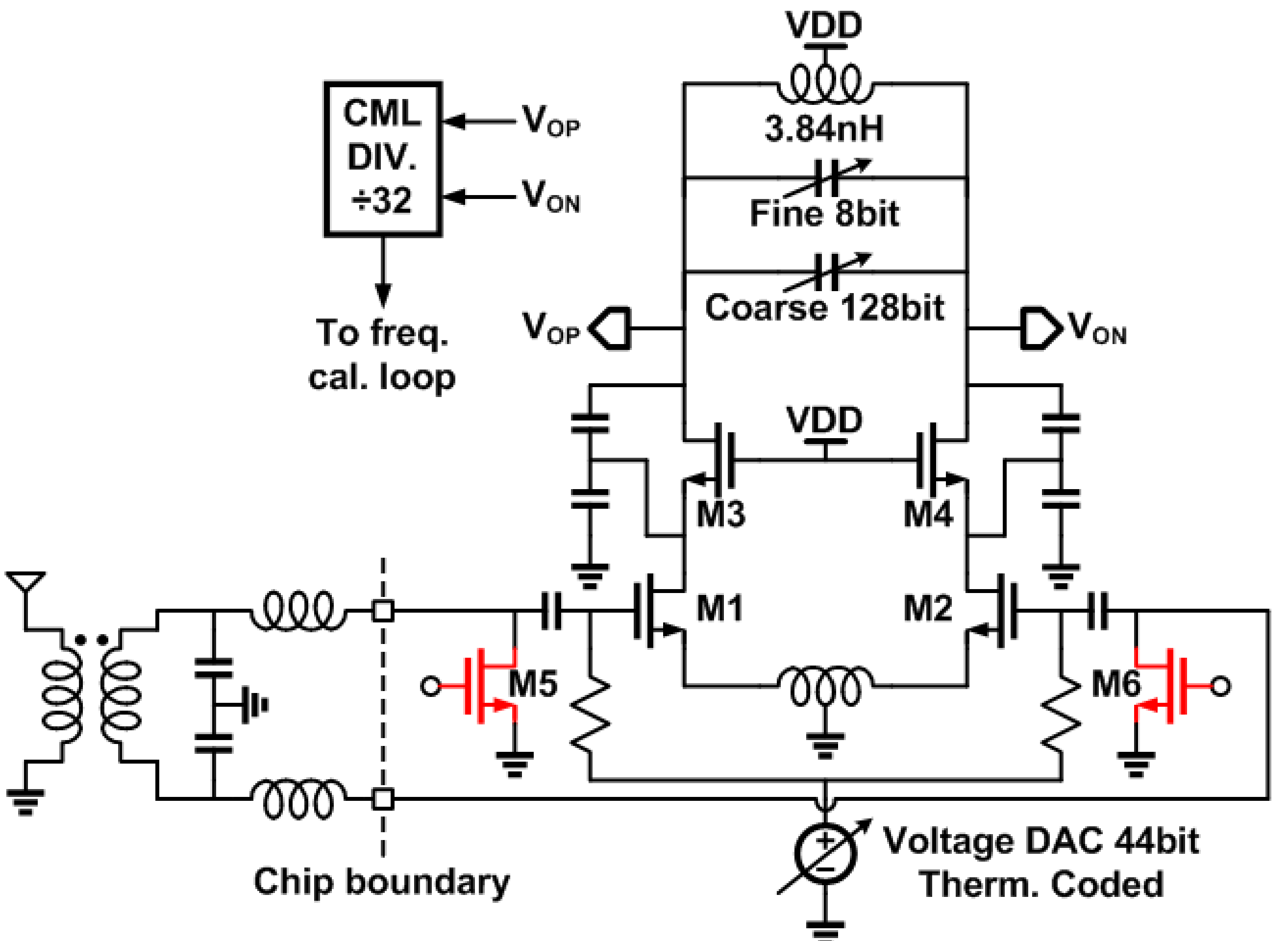
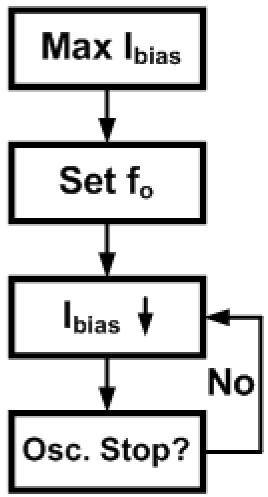




Calibration method



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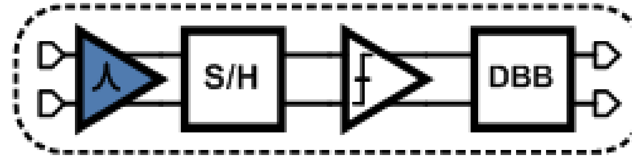
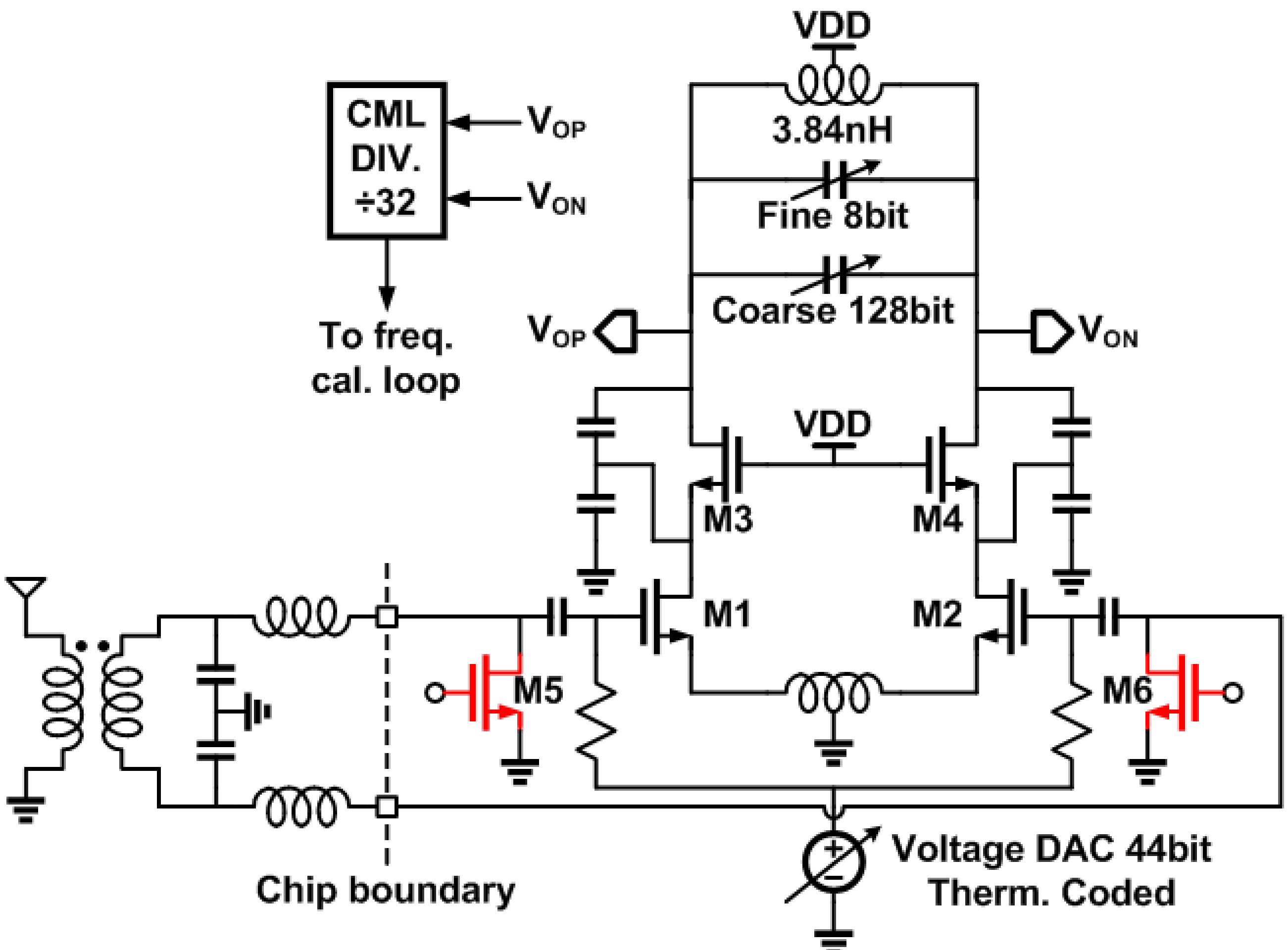
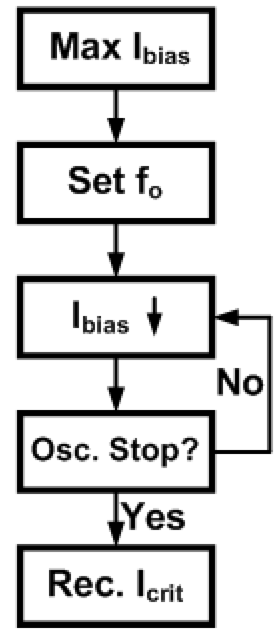




Calibration method



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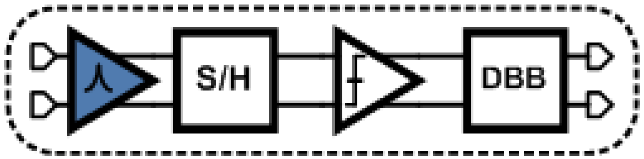
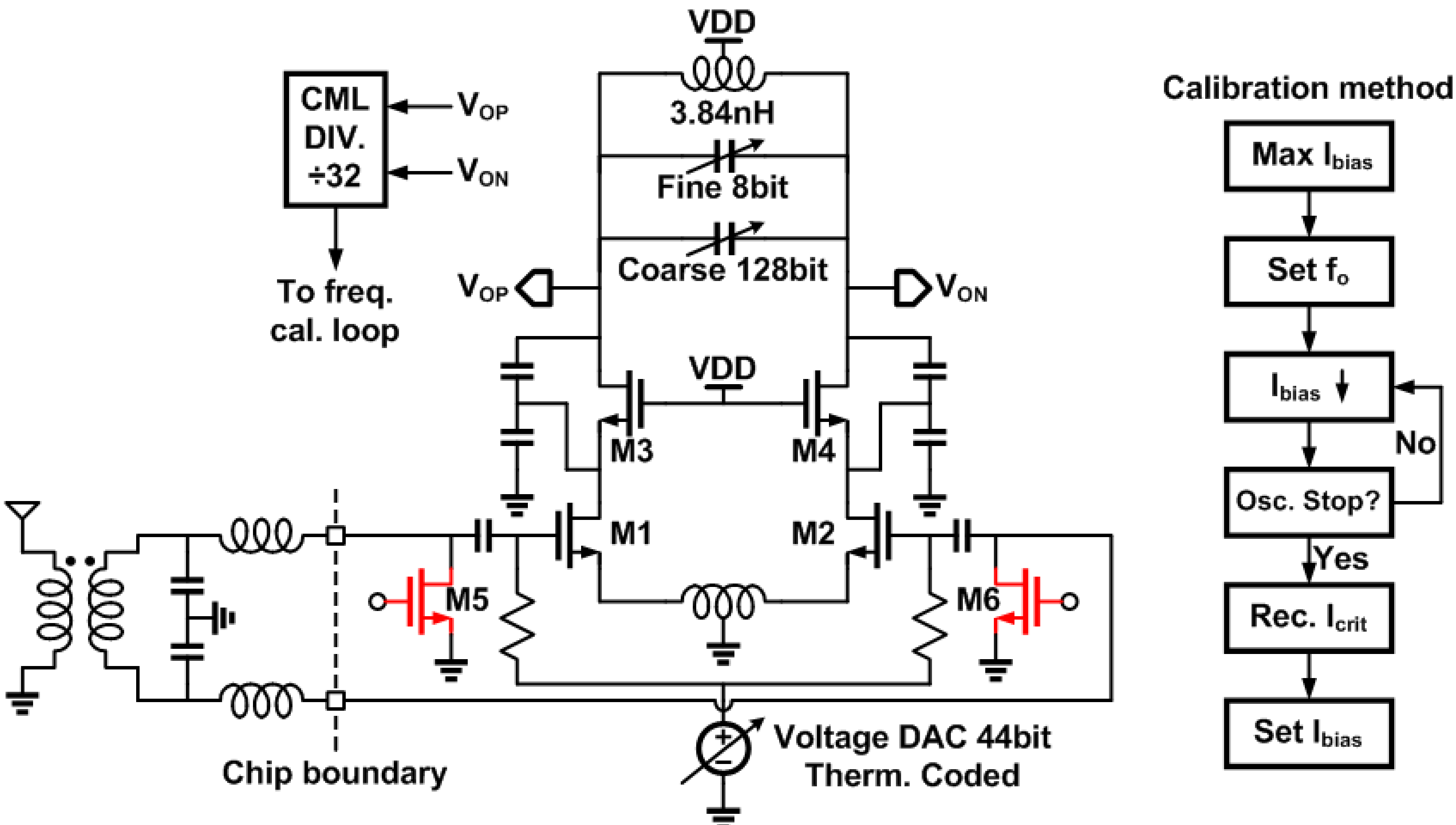
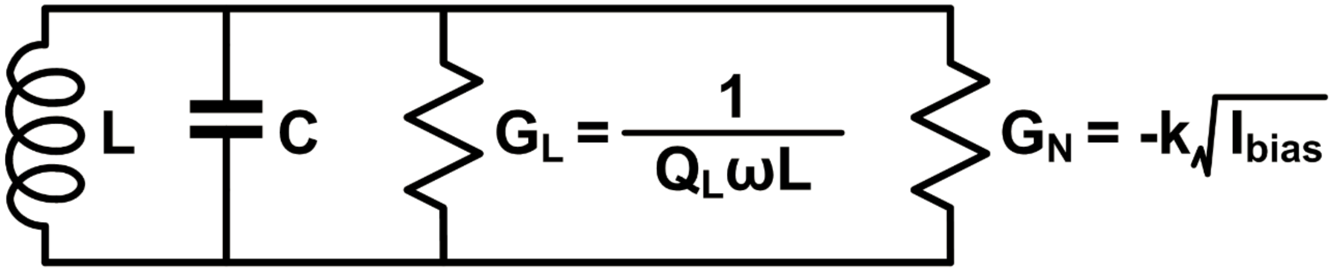
- Calibration facilitates high-Q operation

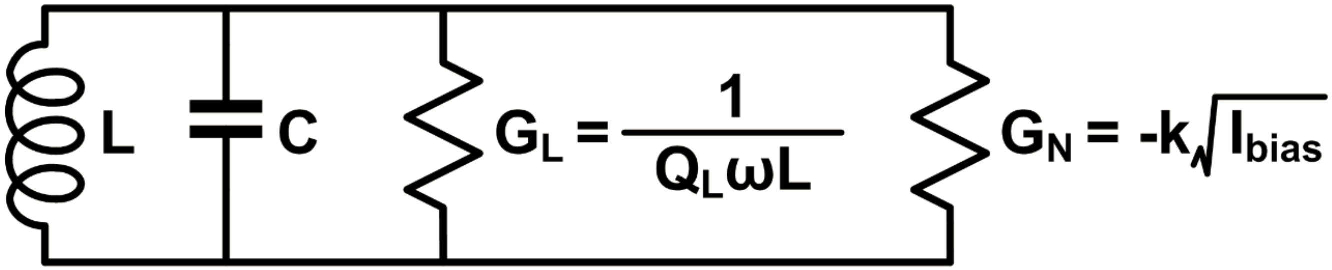




Circuits | Q-Enhancement in LNA



Circuits | Q-Enhancement in LNA

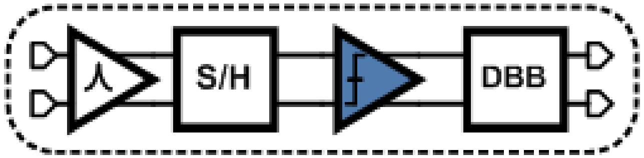


$$\frac{I_{bias}}{I_{crit}} = \left(1 - \frac{Q_L}{Q_{eq}}\right)^2$$

where I_{crit} is the bias current when the negative admittance exactly cancels the intrinsic loss of the tank

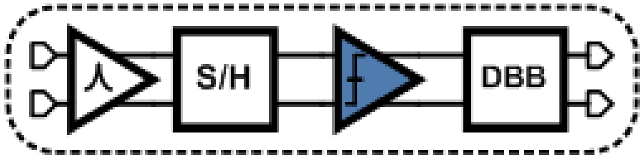
I_{bias} / I_{crit}	Q_{eq}
75%	112
80%	142
85%	192
90%	292
Simulated Q_L = 15	

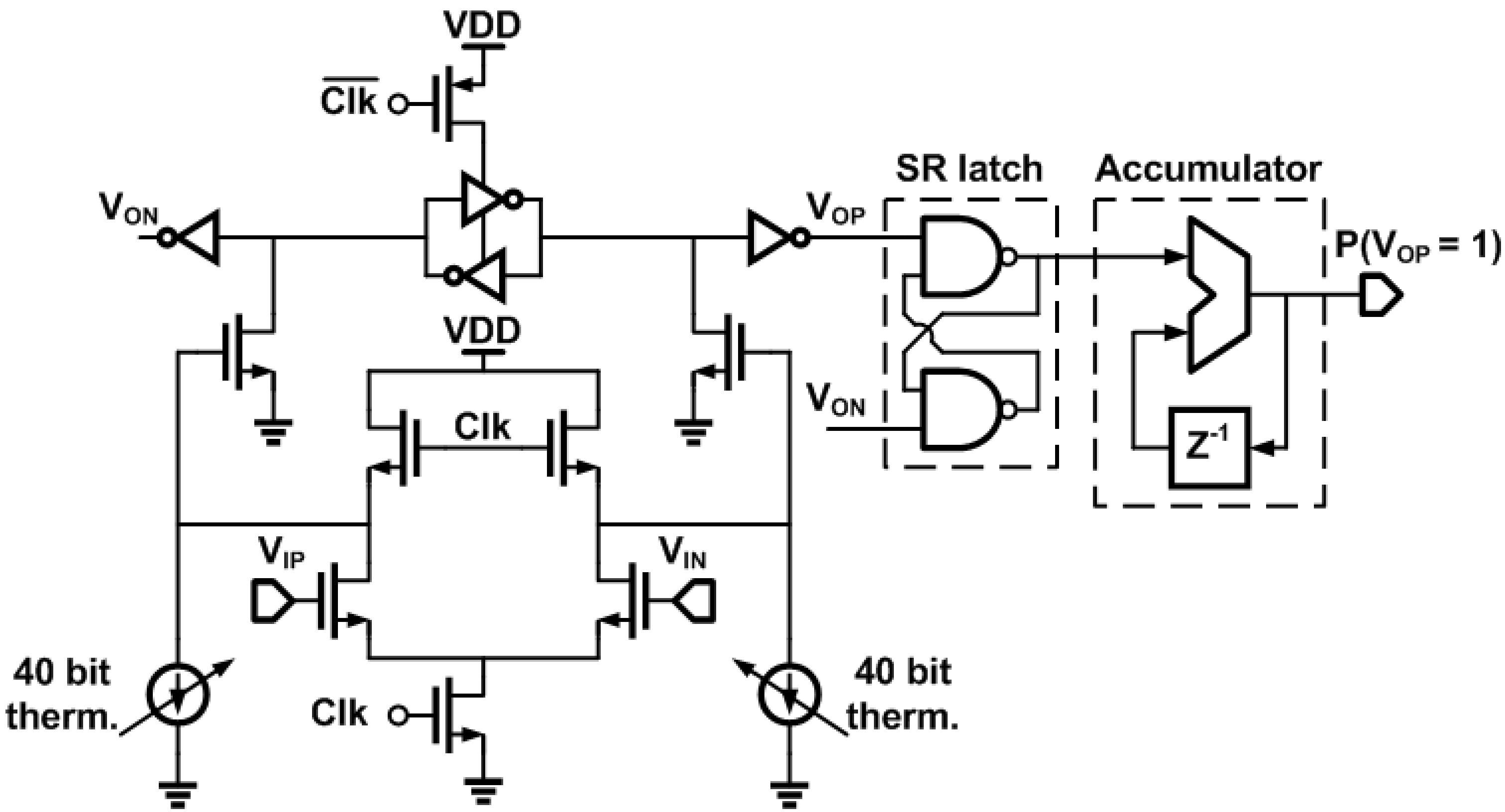
Circuits | 1-b Quantizer



Circuits | 1-b Quantizer

- DC offset calibration [2] to accommodate the small signal amplitude at the quantizer input
- 2-stage architecture for better isolation





[2] Ming-Ju Edward Lee et al., *ISSCC Dig. Tech Papers*, pp. 252-253, Feb. 2000.

Circuits | 1-b Quantizer

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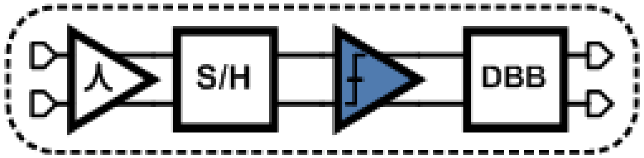

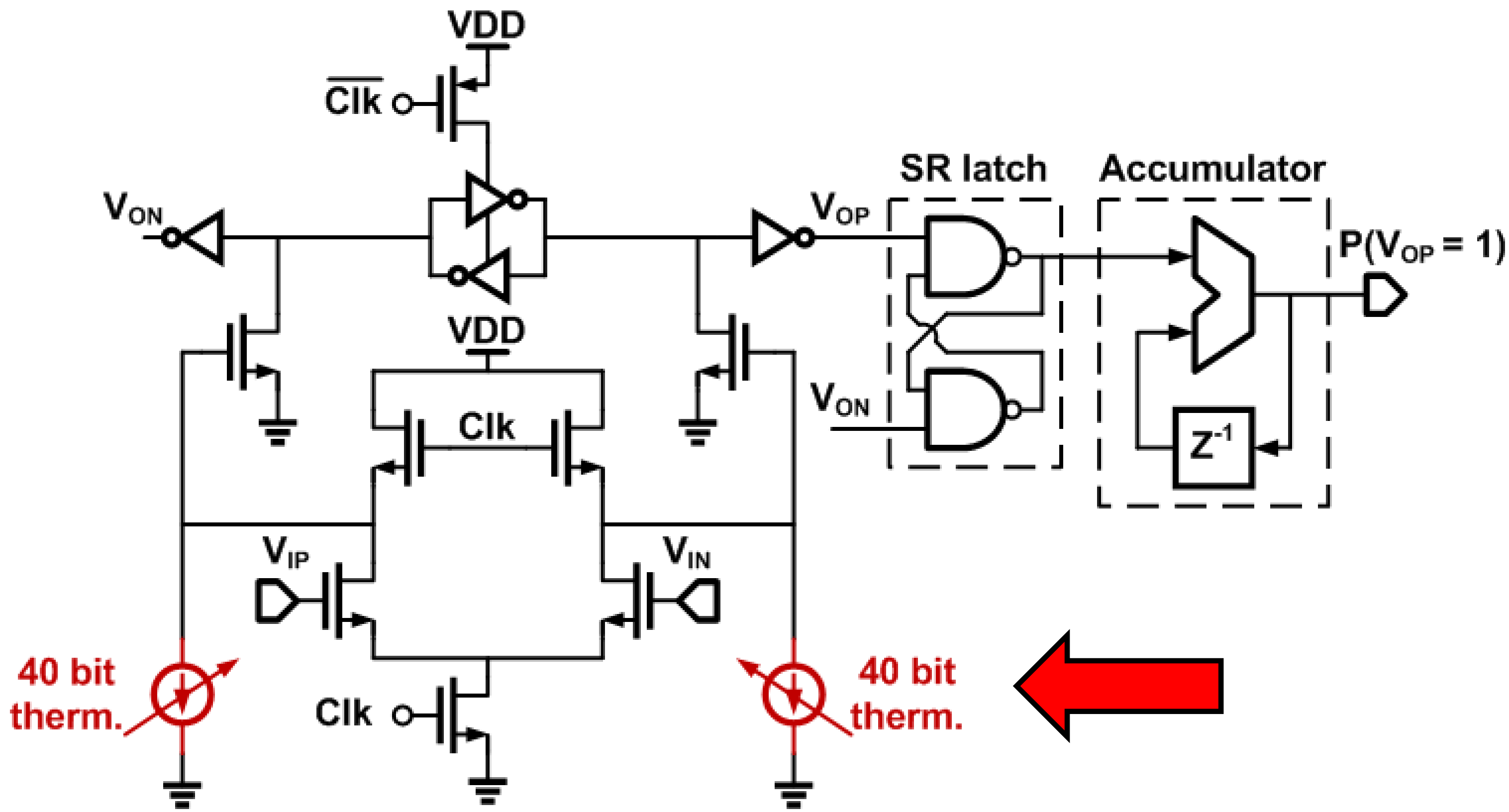

[2] Ming-Ju Edward Lee et al., *ISSCC Dig. Tech Papers*, pp. 252-253, Feb. 2000.

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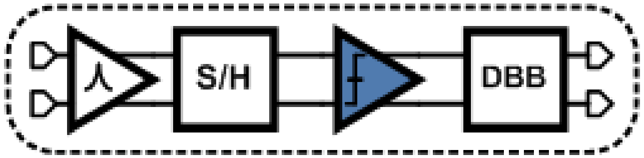

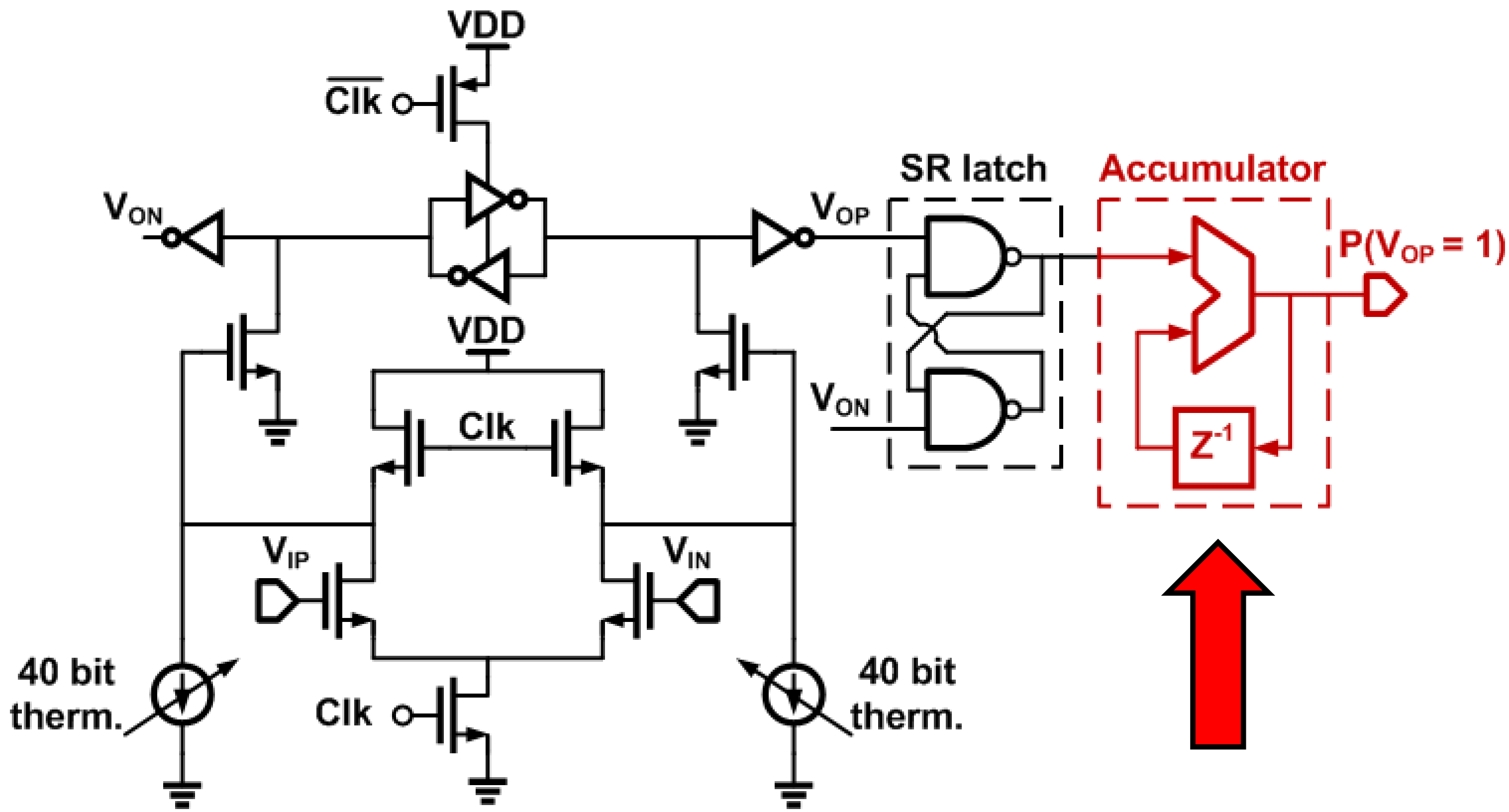

[2] Ming-Ju Edward Lee et al., *ISSCC Dig. Tech Papers*, pp. 252-253, Feb. 2000.

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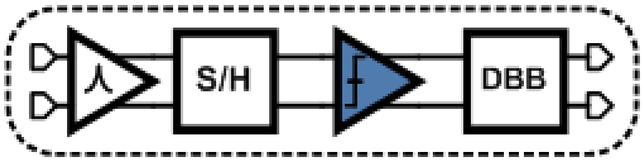
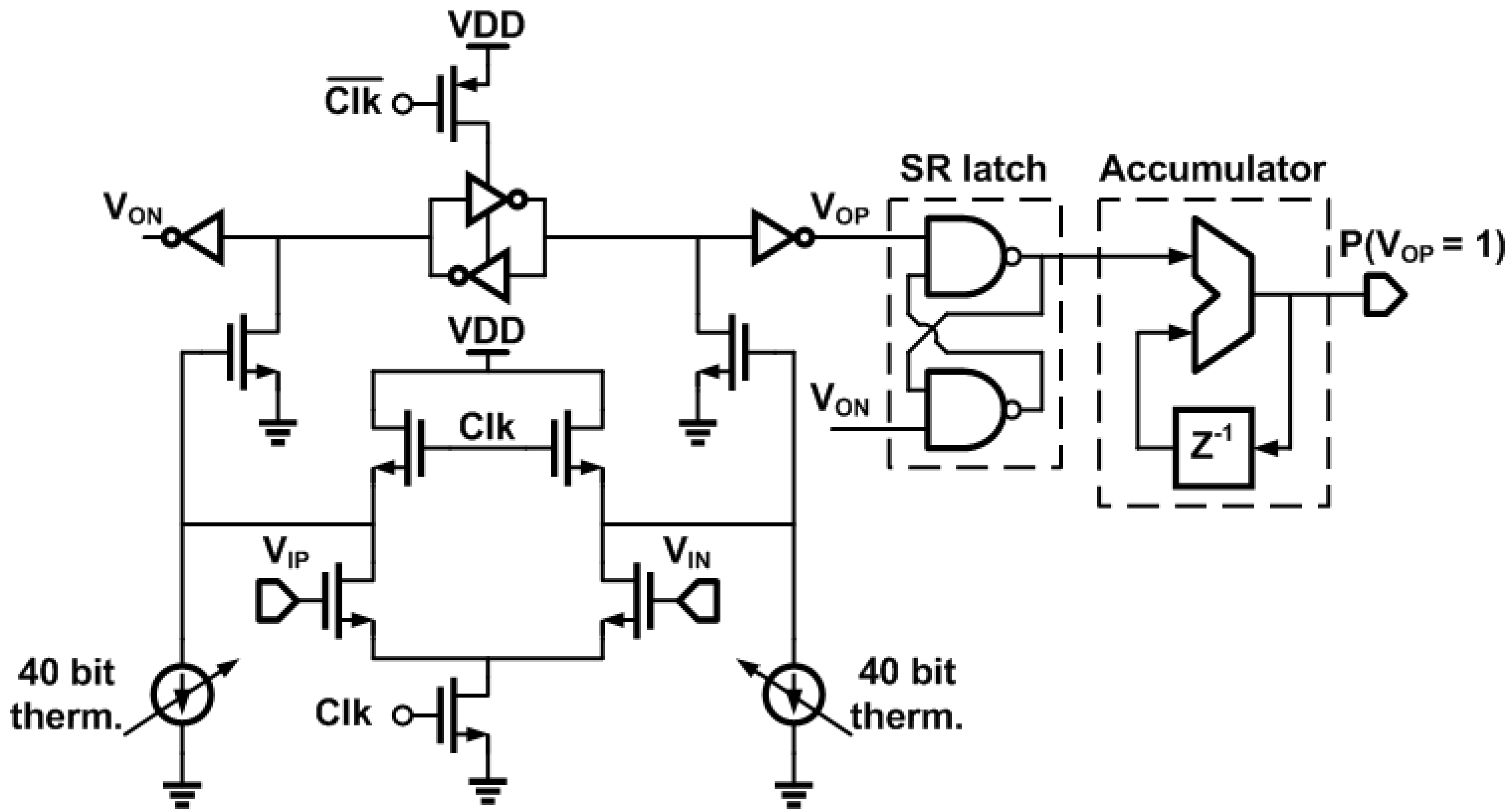
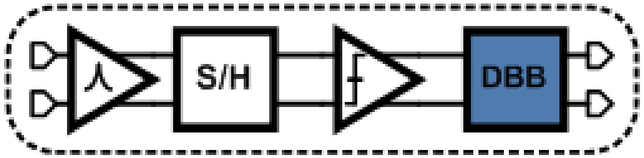


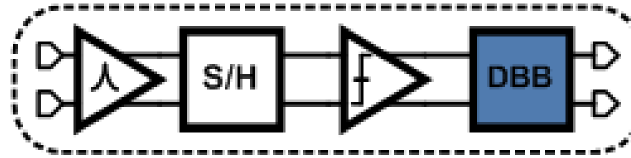


[2] Ming-Ju Edward Lee et al., *ISSCC Dig. Tech Papers*, pp. 252-253, Feb. 2000.

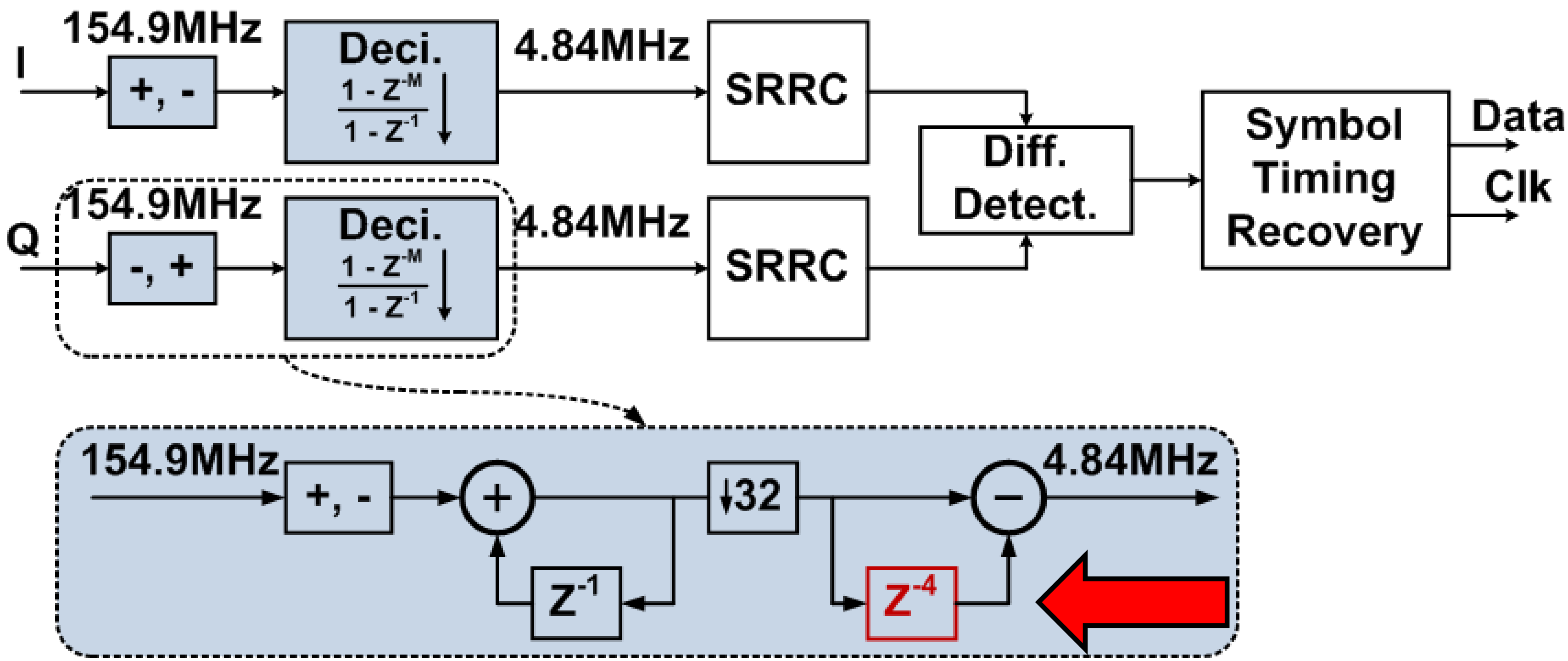
Circuits | Digital IF & Baseband



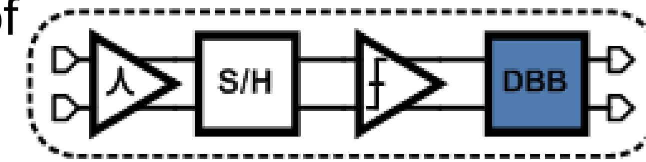
Circuits | Digital IF & Baseband

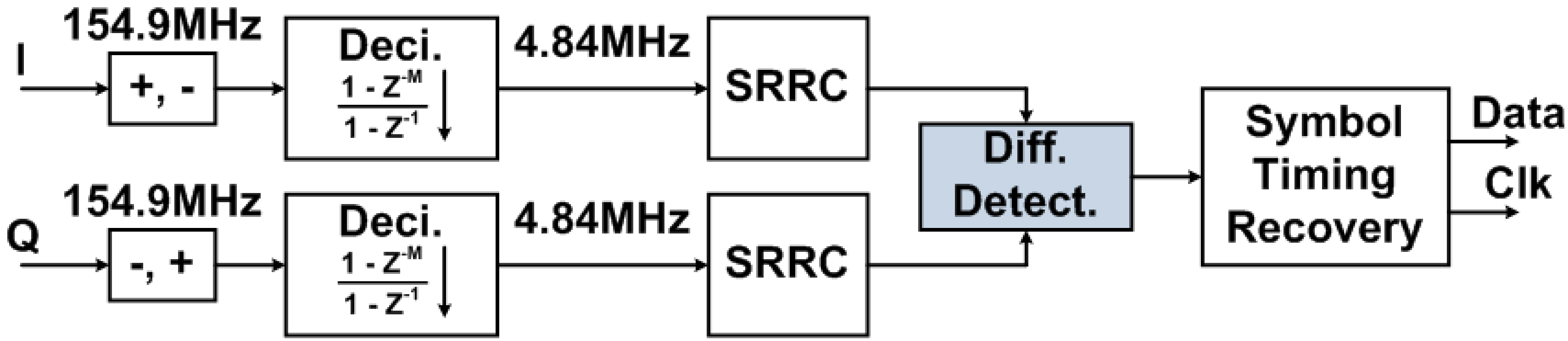


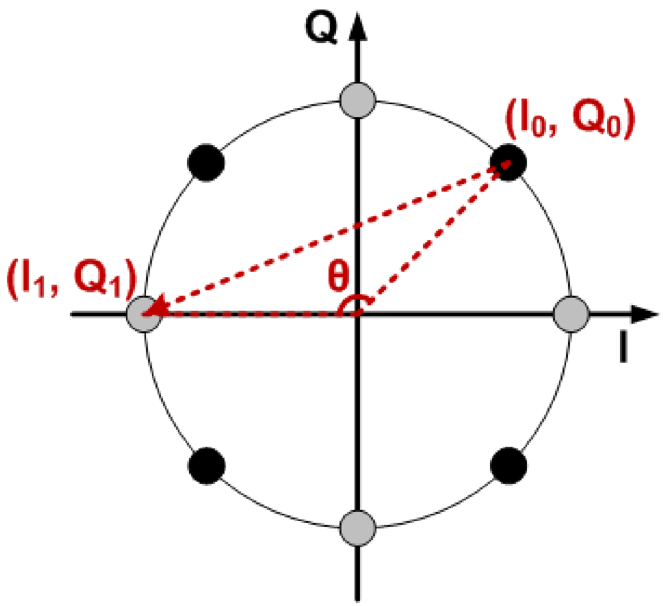
- Modified CIC filter for decimation
  - Averaging length is 128 (ω_{3dB} ~ 600kHz)
  - Down-sampling rate is 32, providing adequate data-transition timing resolution for symbol timing recovery



- Differential detection requires only the signs of cosθ & sinθ, reducing hardware complexity





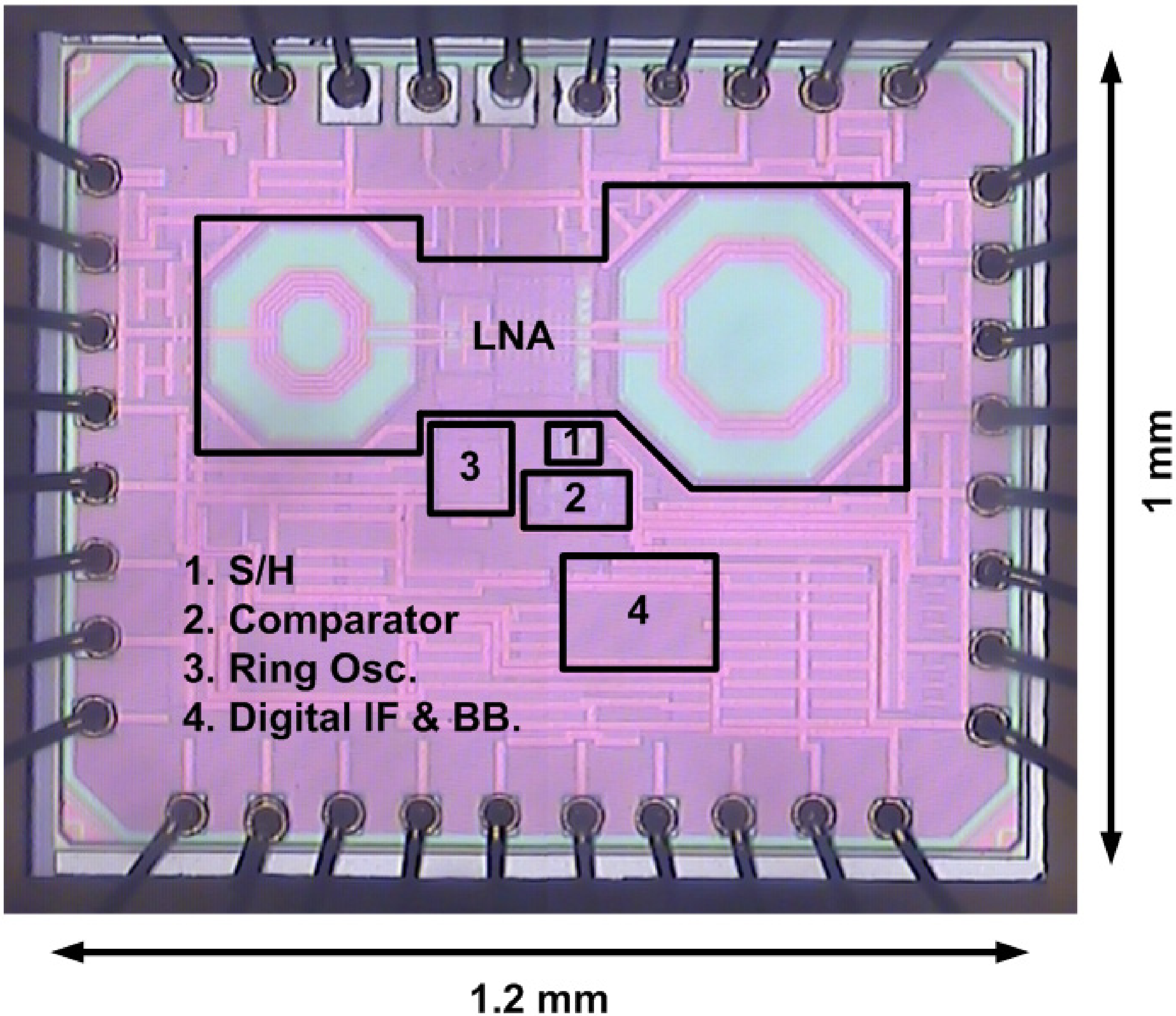


θ	b_{2n}	cosθ	b_{2n+1}	sinθ
π/4	0	>0	0	>0
3π/4	1	<0	0	>0
-3π/4	1	<0	1	<0
-π/4	0	>0	1	<0

$$\mathrm{sign}(\cos\theta) = \mathrm{sign}(I_1 I_0 + Q_1 Q_0)$$

$$\mathrm{sign}(\sin\theta) = \mathrm{sign}(Q_1 I_0 - I_1 Q_0)$$

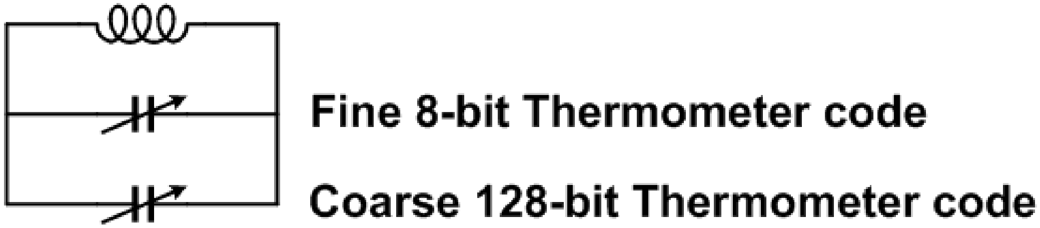
Die Photo

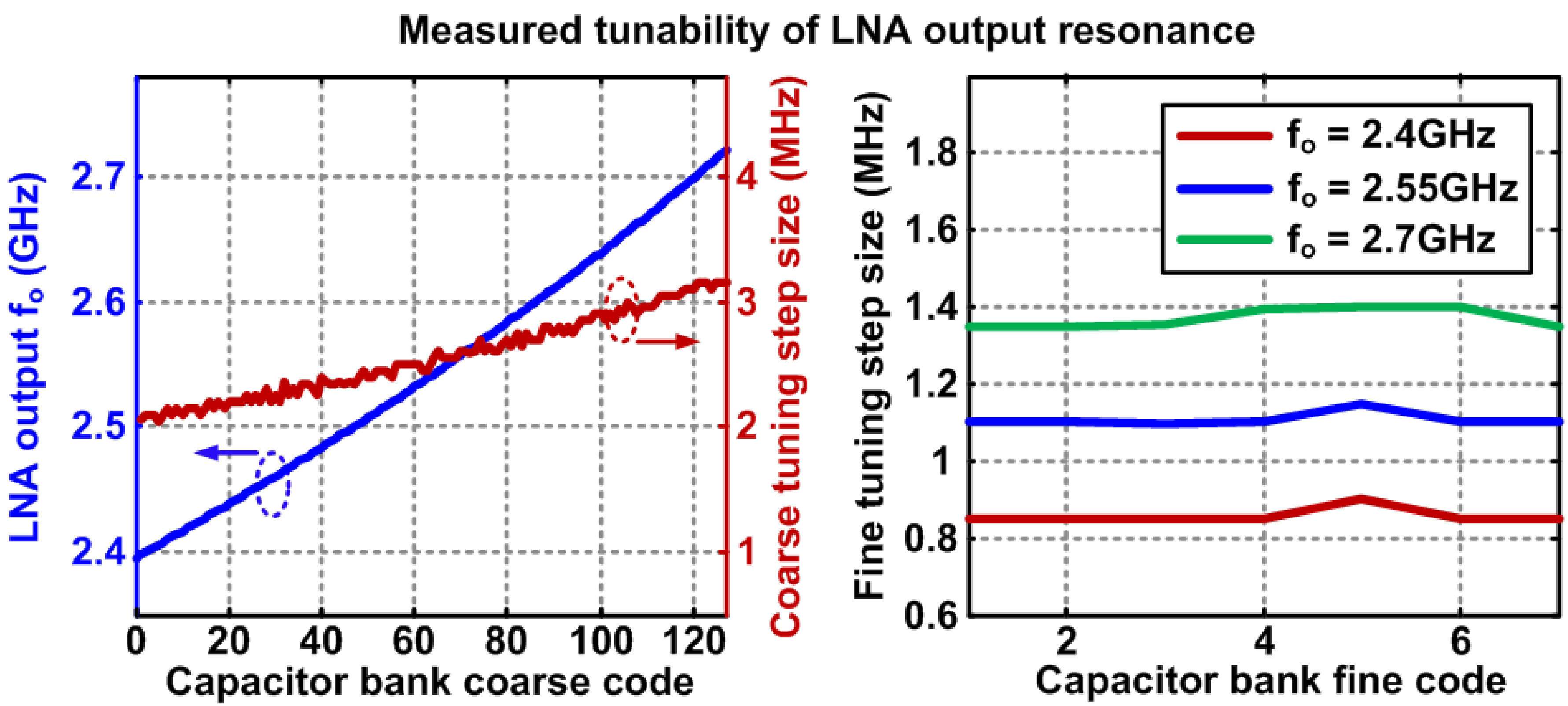


Measurement

Measured Tunability of LNA Output Resonance

- LSB is 1.4MHz, sufficient for operation with Q enhanced to 900

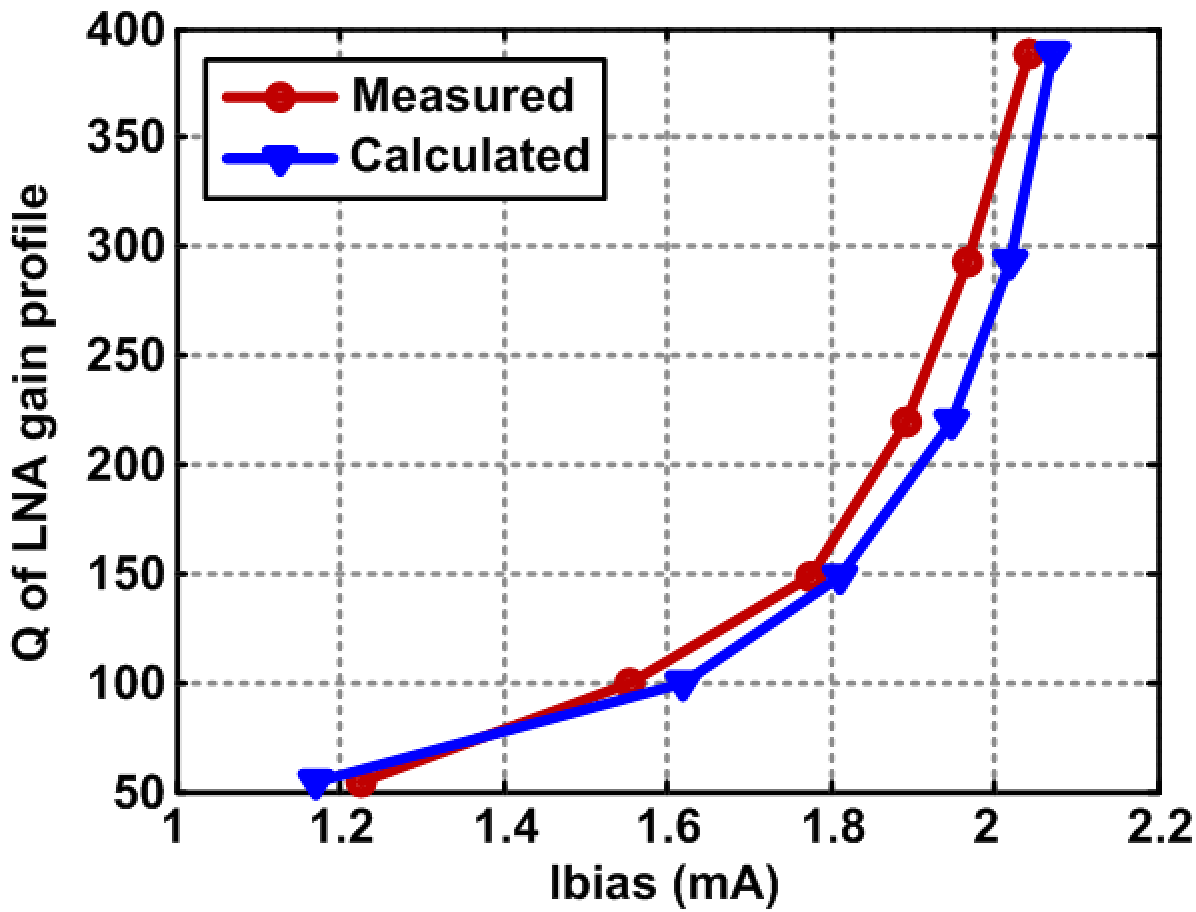




Measured Q-Enhancement Performance

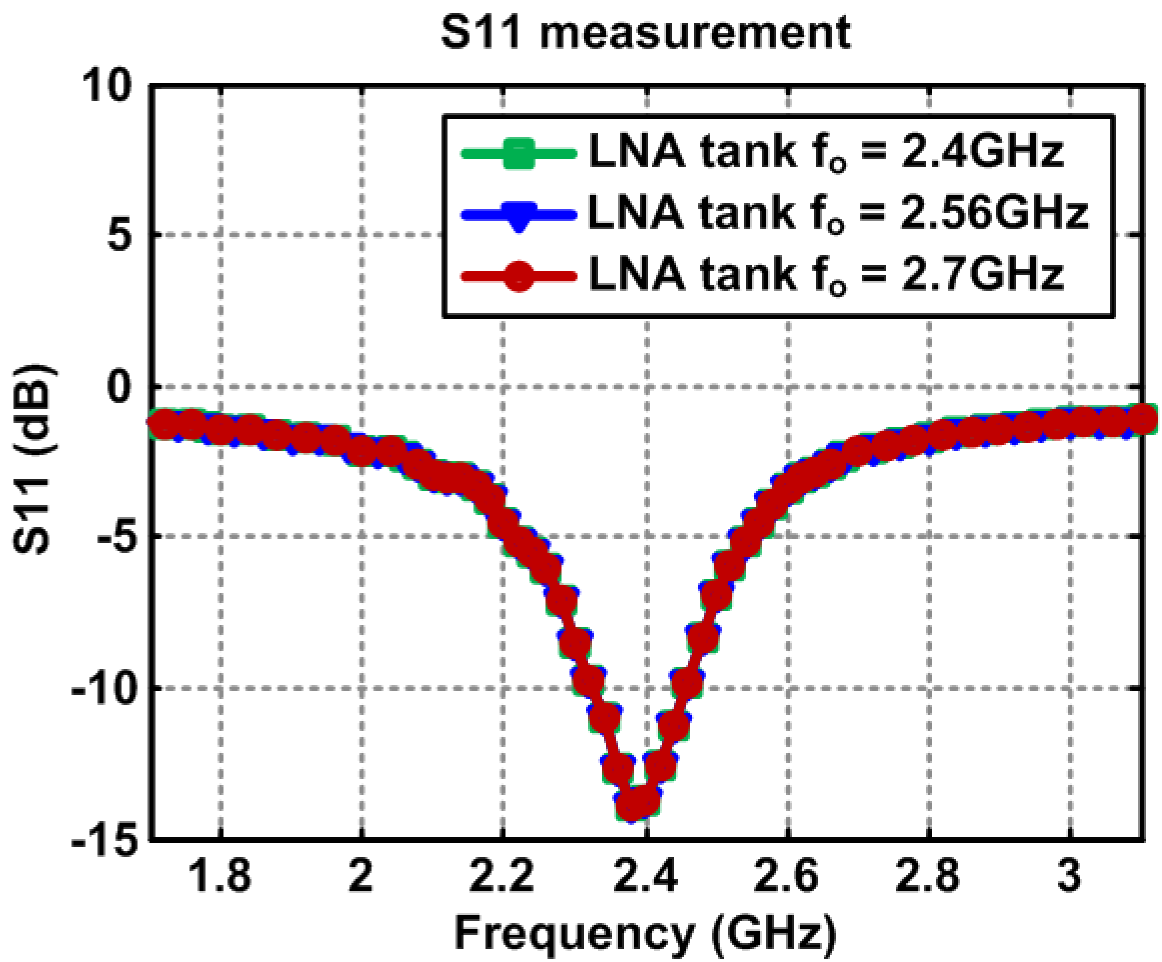
- Q can be enhanced up to 400 in measurement
- Q with enhancement can be set from 60 to 400 with step size of ~70

$$\frac{I_{bias}}{I_{crit}} = \left(1 - \frac{Q_L}{Q_{eq}}\right)^2$$



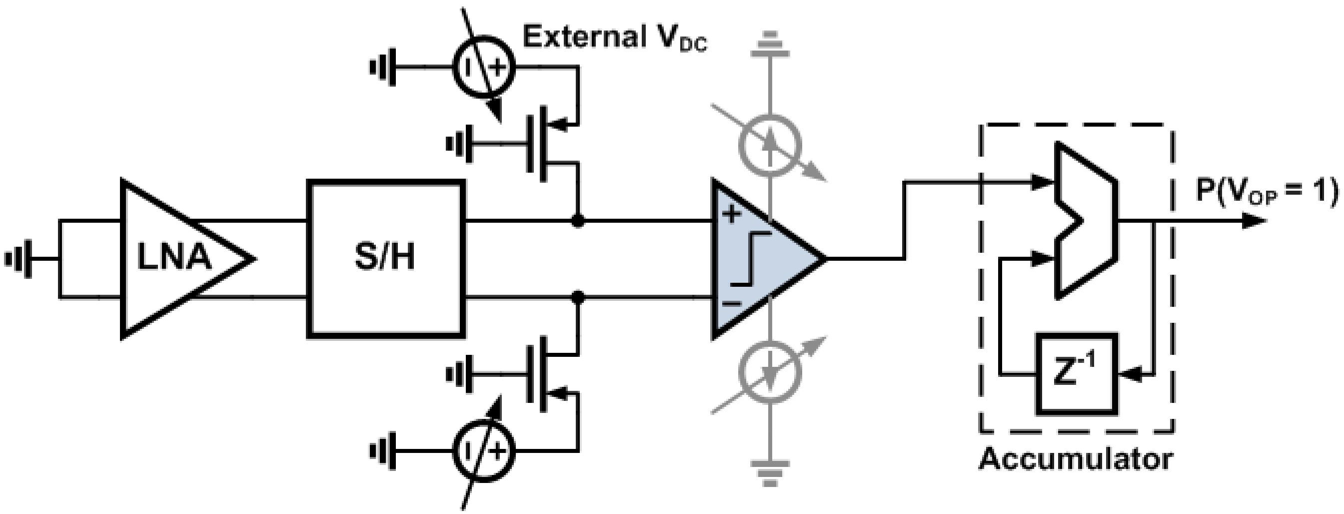
Measured Input Matching

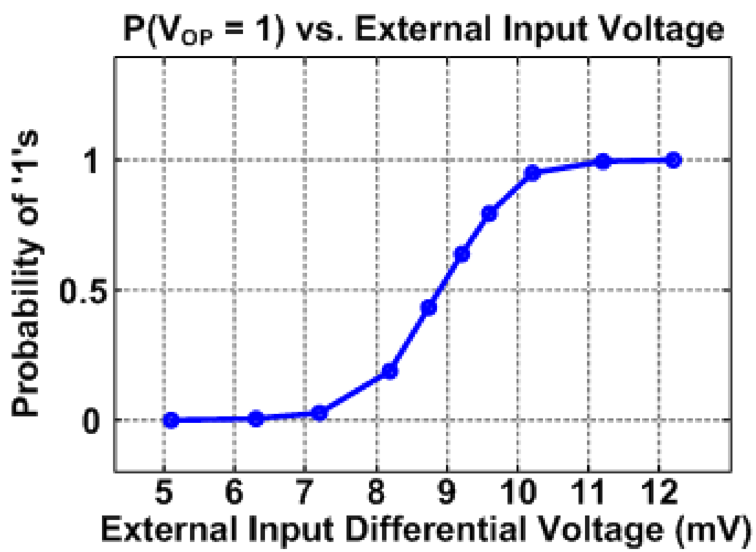
- Input matching and LNA calibration can be performed independently



1-b Quantizer Measurement

- Quantizer DC offset is measured by external DC voltage sources

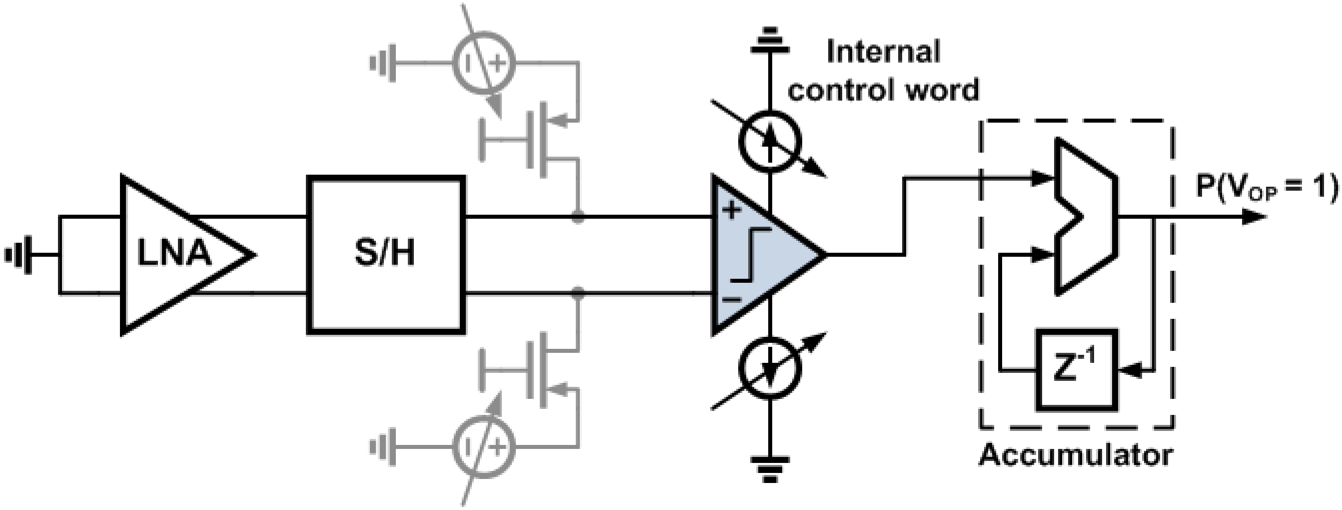


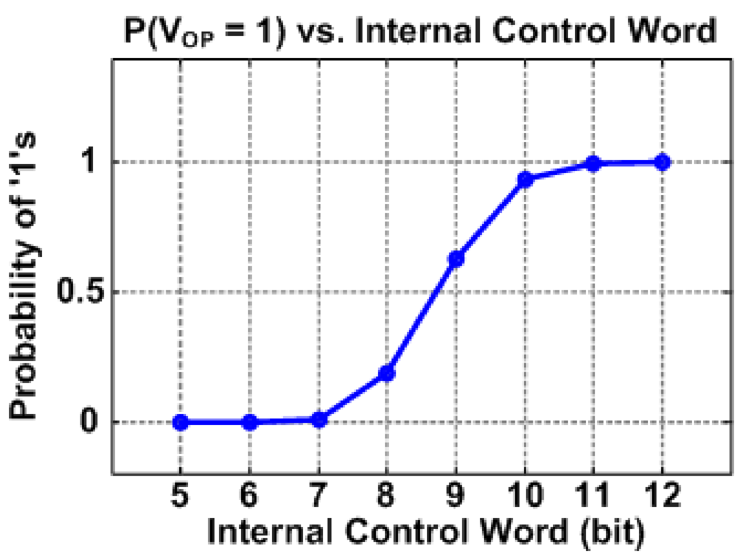


- DC offset = 8.9mV
- Noise σ = 0.88mV

1-b Quantizer Measurement

- Quantizer DC offset is calibrated on-die

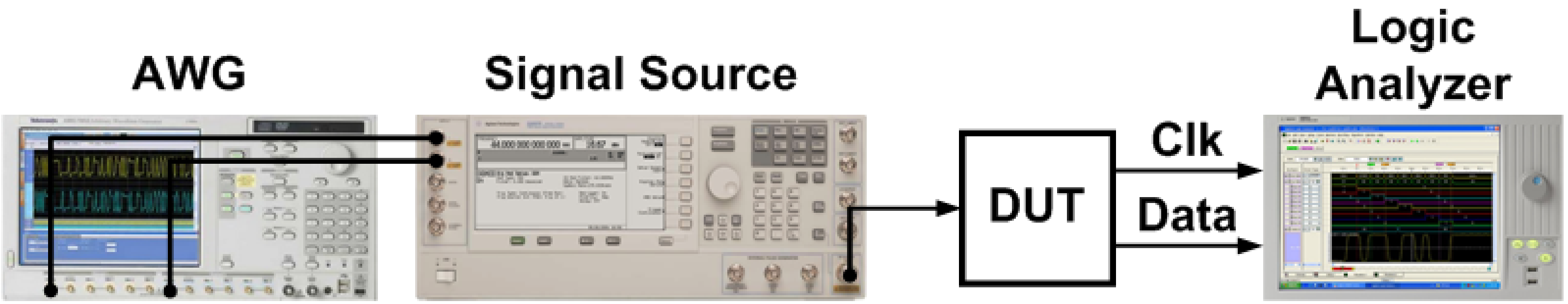


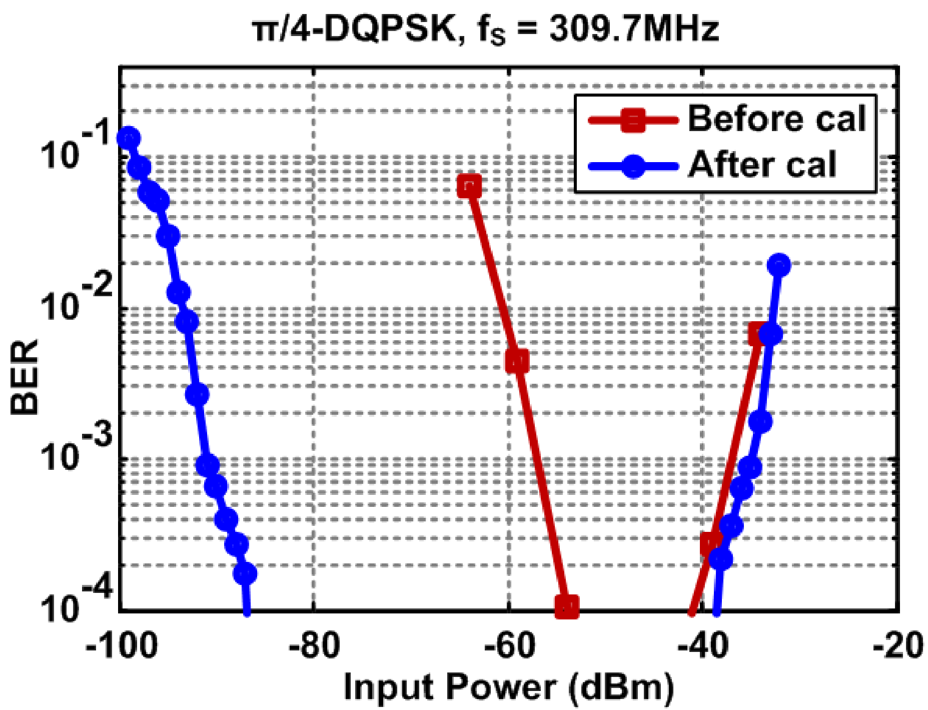


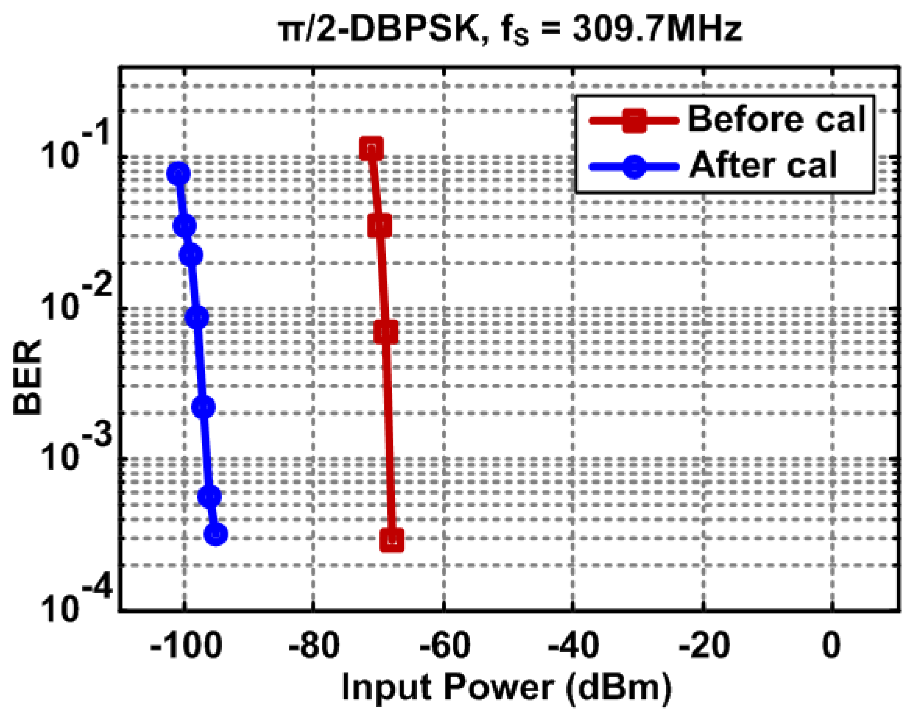
- Calibration step is ~1.02mV, yielding a worst case offset residue of ~0.51mV

Bit Error Rate Measurement

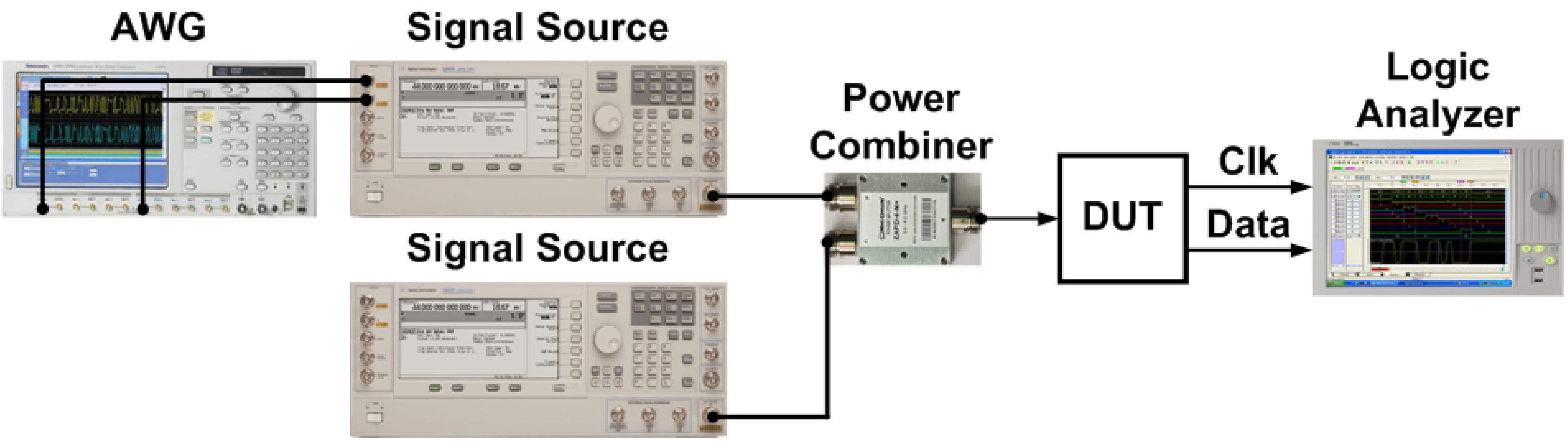
- BERs are measured before and after on-die DC offset calibration

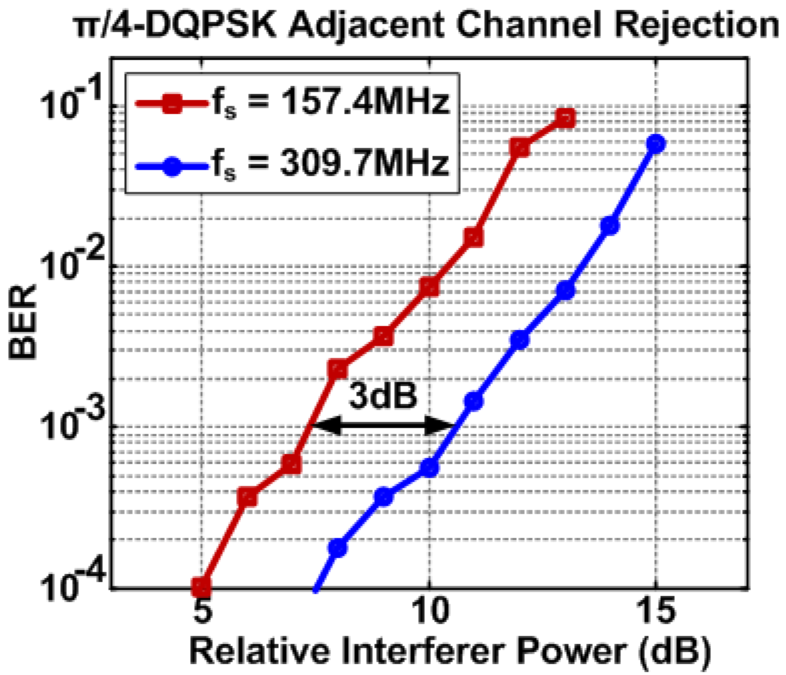


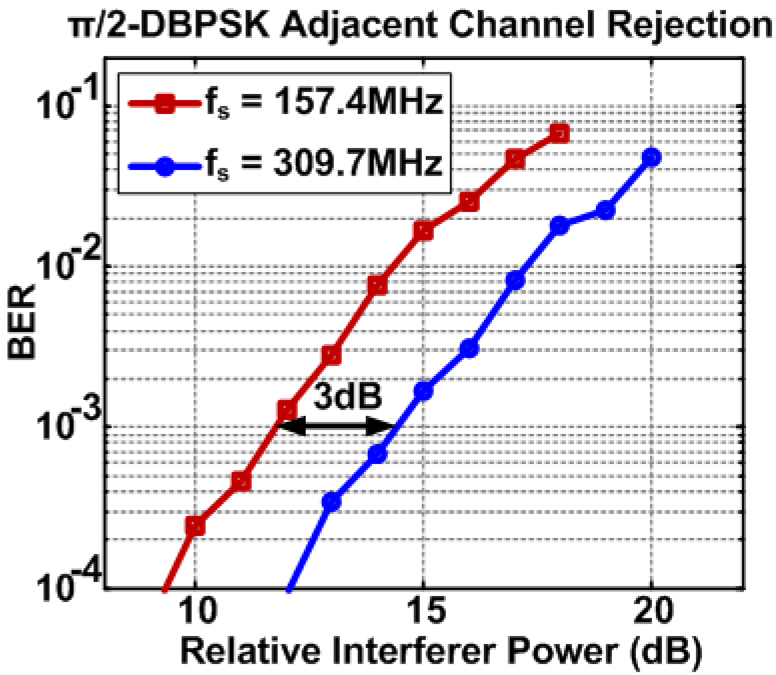




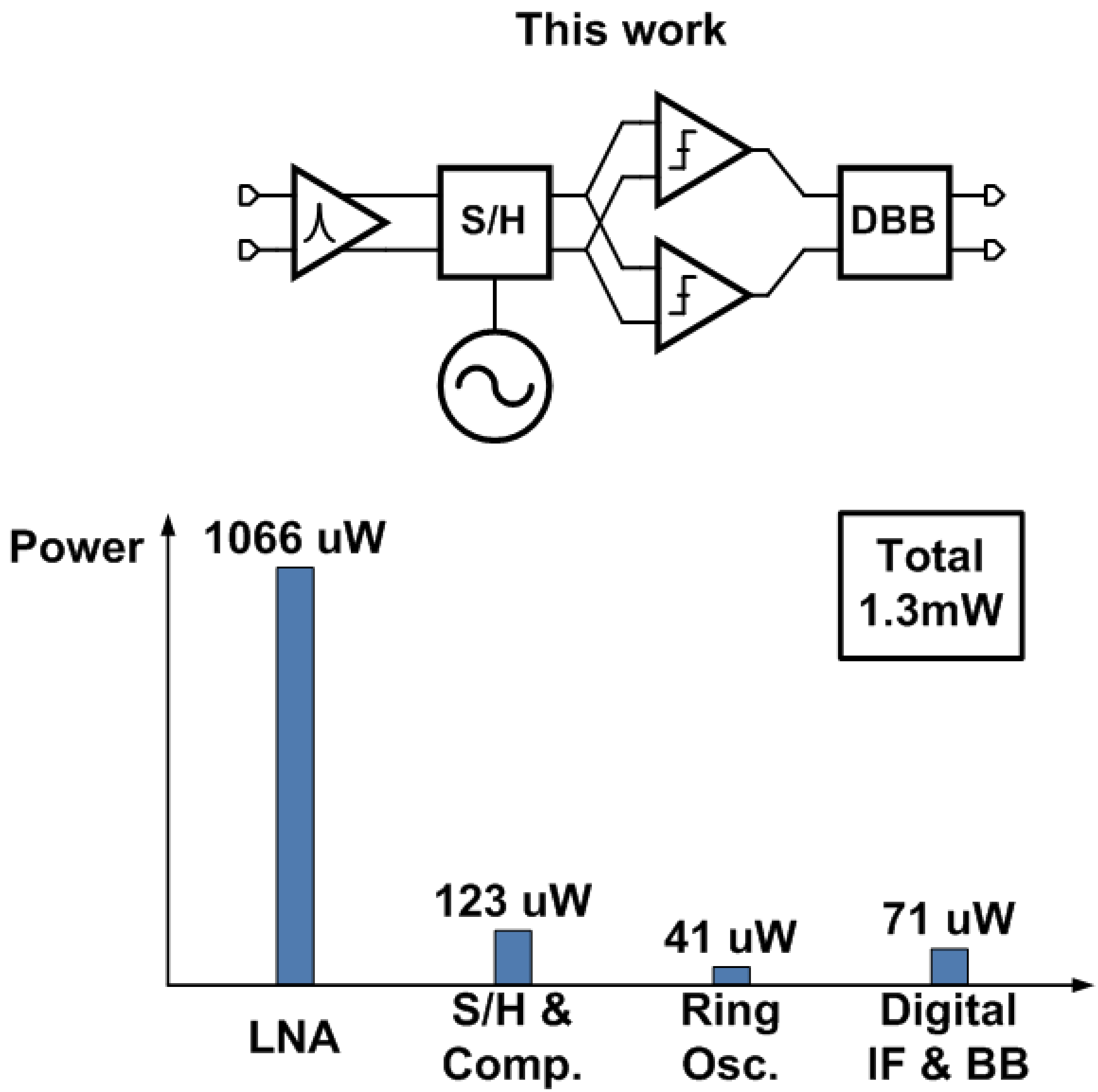
Adjacent Channel Rejection Measurement





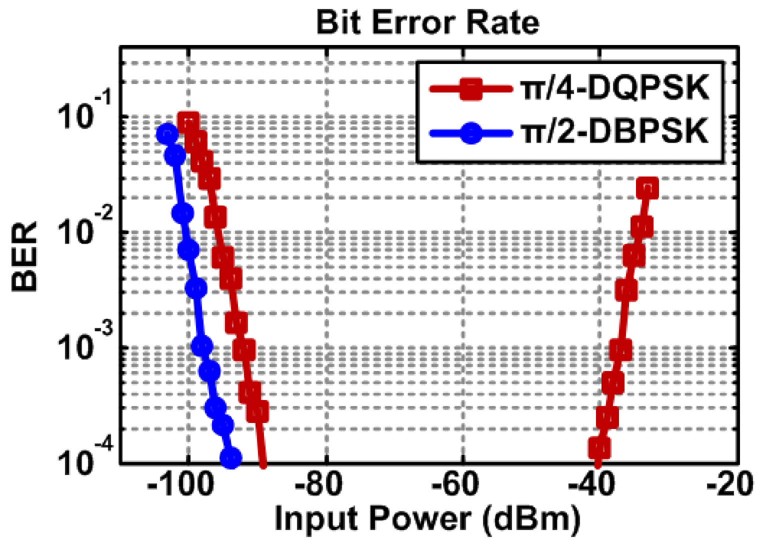


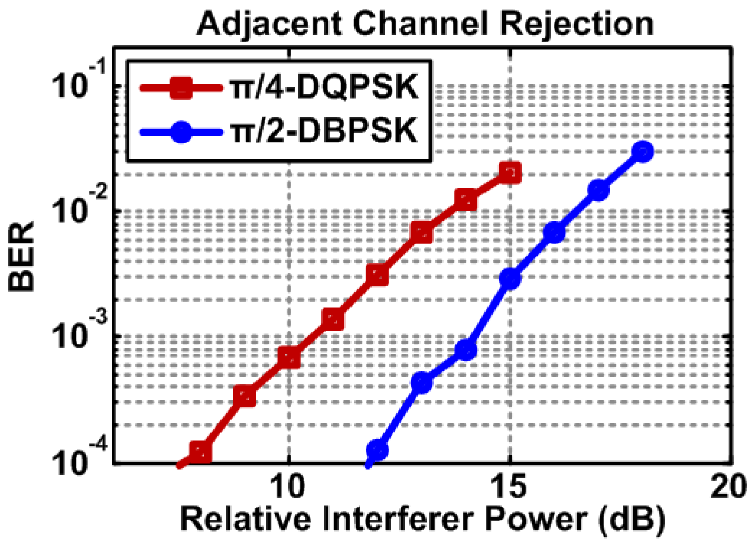
Power Breakdown

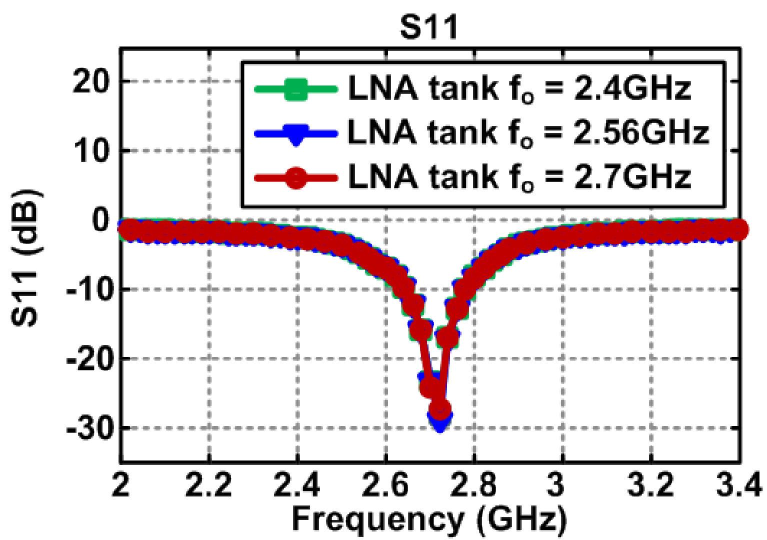


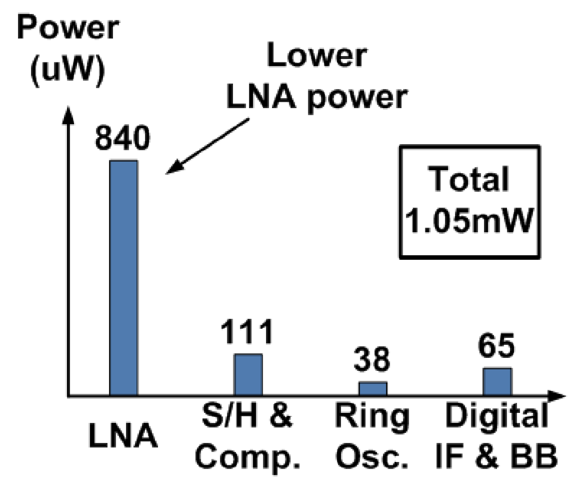
2.7GHz Measurement Summary

- Highest intrinsic Q achieved at 2.7GHz when all bank caps switched off









Performance Summary and Comparison

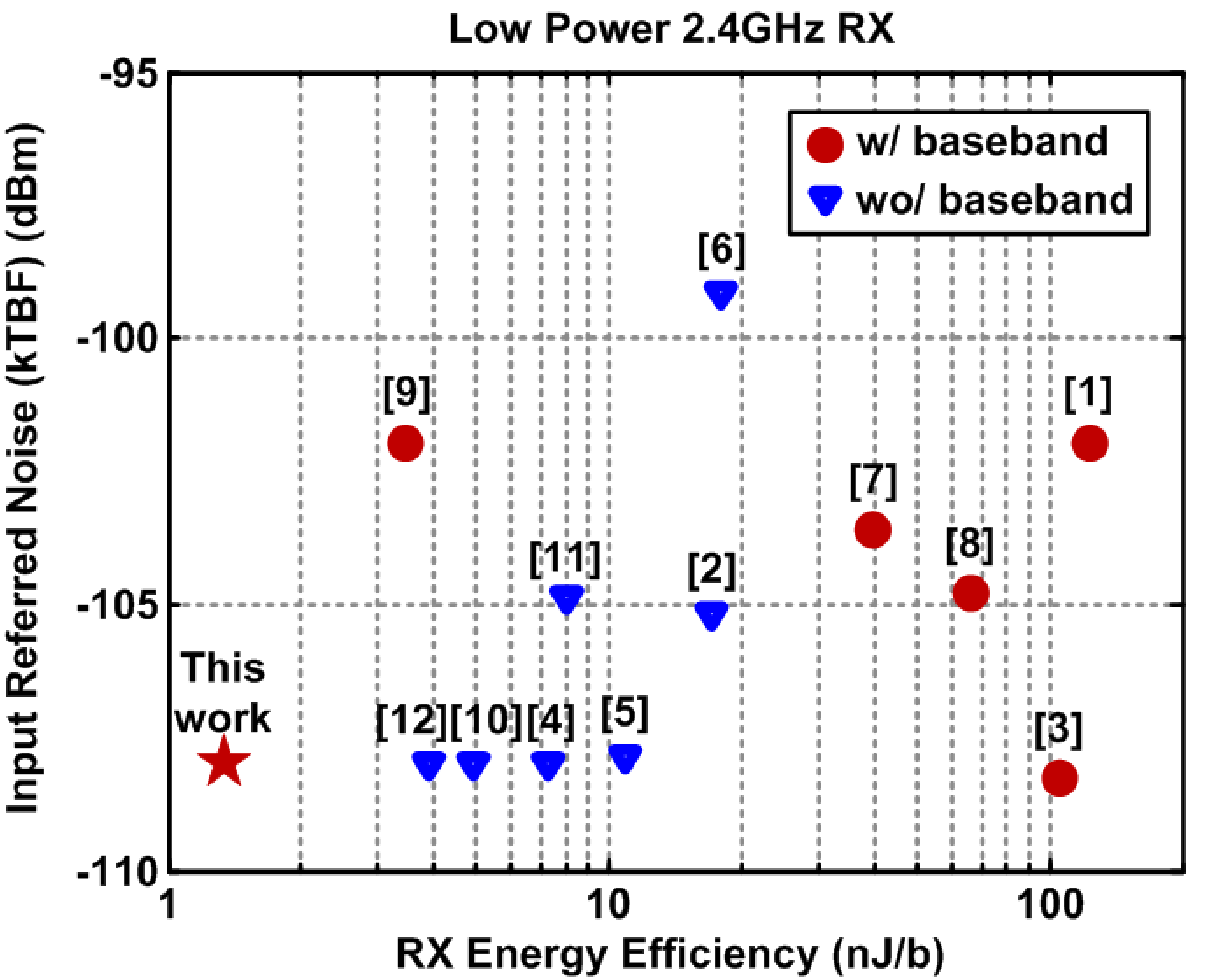
	This work		ISSCC 13 [1]	ISSCC 12 [3]	ISSCC 13 [4]
RX architecture	Sub-sampling		Sliding IF	Sliding IF	Low IF
Modulation	π/2-DBPSK / π/4-DQPSK		π/4-DQPSK	π/2-DBPSK / π/4-DQPSK	BFSK
Data rate	486 kbps / 971 kbps		971 kbps	121 kbps / 971 kbps	200 kbps
Frequency band	2.4 GHz	2.7 GHz	2.4 GHz	2.4 GHz	2.46 GHz
Noise figure	6 dB	5 dB	6 dB	6 dB	6.1 dB
Sensitivity	-96 / -91 dBm (0.1% BER)	-97 / -92 dBm (0.1% BER)	-96 dBm (10% PER)	-104 dBm / -96.5 dBm (10% PER)	-91.5 dBm (0.1% BER)
Active / die area	**0.35 / 1.2 mm^2 (65nm)**		**2 / 3.7 mm^2 (90nm)**	**- / 5.9 mm^2 (130nm)**	**- / 2.5 mm^2 (65nm)**
Supply	**0.6 V**		**1.2 V**	**1 V**	**0.3 V**
Power dissipation	**1301 uW**	**1054 uW**	**3.8 mW [1]**	**4.8 mW [2]**	**1.6 mW [1,2]**
RX energy effi.	**1.34 nJ/b**	**1.09 nJ/b**	**3.9 nJ/b**	**4.9 nJ/b**	**8 nJ/b**
RX FOM [3]	**227 dB**	**228 dB**	**222 dB**	**221 dB**	**216 dB**

1. Power dissipation excluding digital baseband
2. Power dissipation excluding ADC / off chip drivers
3. RX FOM = - 10*log(kTBF) - 10*log(P_{DC}/Data rate), based on [1]

[1] Yao-Hong Liu et al., *ISSCC Dig. Tech Papers*, pp. 446-447, Feb. 2013.
[3] Alan Wong et al., *ISSCC Dig. Tech Papers*, pp. 300-301, Feb. 2012.
[4] Fan Zhang et al., *ISSCC Dig. Tech Papers*, pp. 456-457, Feb. 2013.

Performance Comparison

- 3x lower power consumption with comparable noise performance



[1] JSSC01
[2] JSSC05
[3] JSSC06
[4] JSSC06
[5] JSSC07
[6] JSSC13
[7] JSSC13
[8] JSSC13
[9] JSSC13
[10] JSSC13
[11] ISSCC13
[12] ISSCC13

Conclusion

- We demonstrate a low-power, low-VDD WBAN receiver:
  - ➢ Sub-sampling
  - ➢ Q-enhancement
  - ➢ Early digitization with 1-b ADC
- The measured WBAN RX achieves:
  - ➢ -91dBm sensitivity for π/4-DQPSK
  - ➢ 1.3mW @ 2.4GHz
  - ➢ 0.35mm^2 active area
- Proposed techniques are applicable to other low-power applications and are compatible with technology scaling

Acknowledgements

• This work was sponsored, in part, by the Center for the Design of Analog-Digital Integrated Circuits (CDADIC), the Catalyst Foundation, and the National Science Foundation (IIP-1127853, IIS-1118017)

A 0.33nJ/b IEEE802.15.6/Proprietary-MICS/ISM Band Transceiver with Scalable Data-Rate from 11kb/s to 4.5Mb/s for Medical Applications

M. Vidojkovic, X. Huang, X. Wang, C. Zhou, A. Ba, M. Lont, Y. Liu
M. Ding, B. Busze, N. Kiyani, K. Philips, H. de Groot
Holst Centre – IMEC, Eindhoven, The Netherlands

P. Harpe
Eindhoven University of Technology, The Netherlands

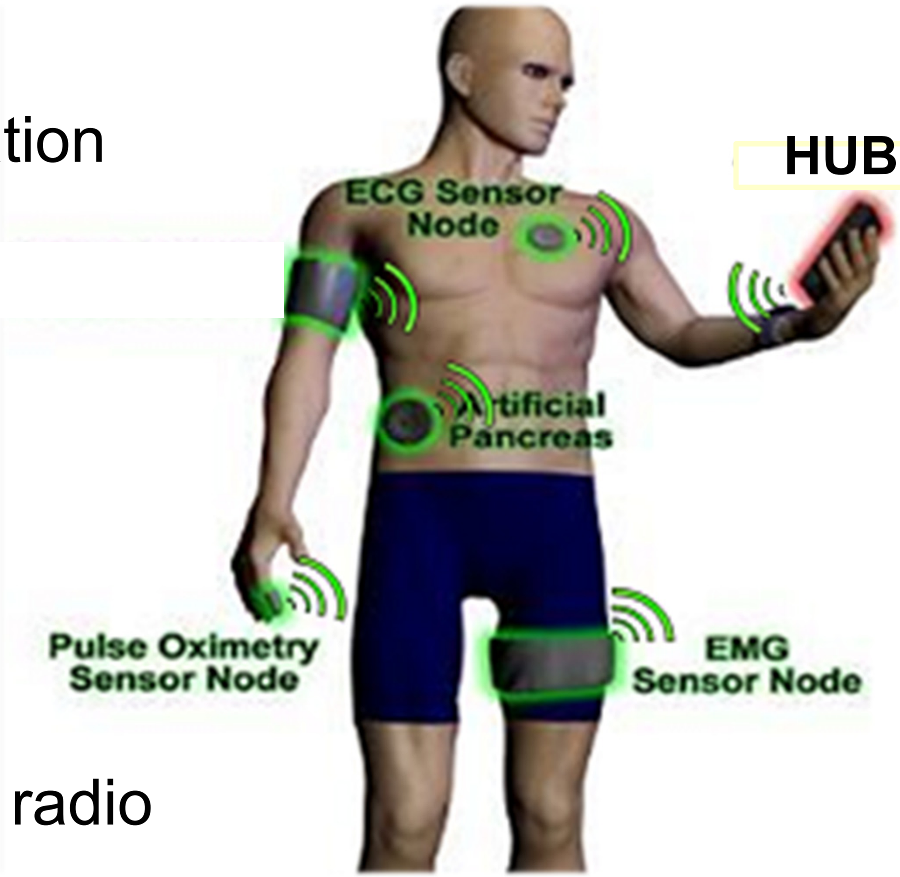
K. Kanda, S. Masui
Fujitsu Laboratories, Kawasaki, Japan

Outline

- Motivation
- Transceiver design challenges
- 400MHz MICS/ISM band transceiver
  - Circuit implementation
  - Measurement results
- Conclusions

Motivation

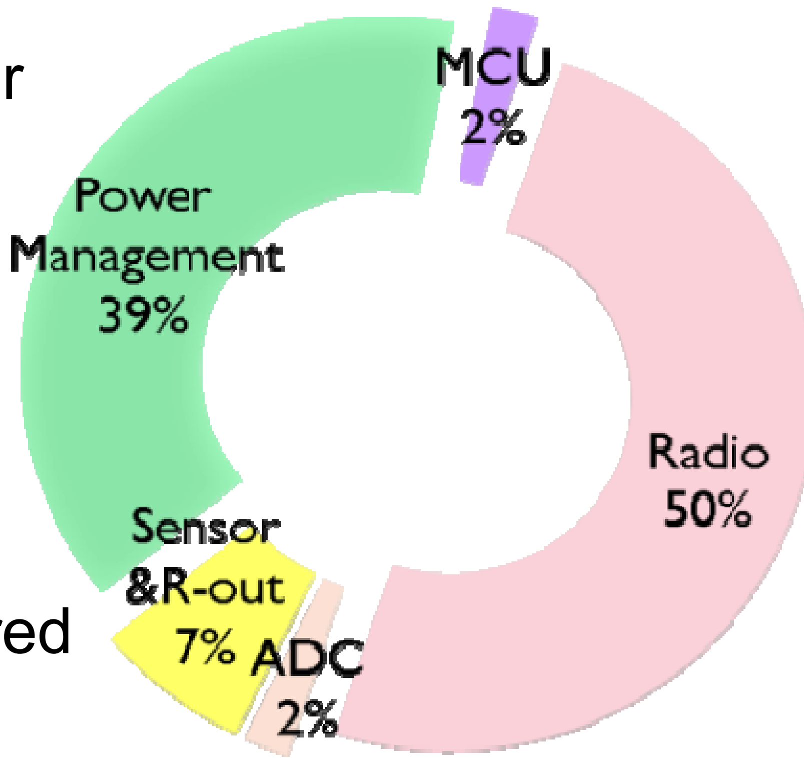
- **IEEE 802.15.6 standard**
  - For short-distance communication in/around human body
  - PHY supports various bands
    - ✓402 - 405MHz (MICS band)
    - ✓420 - 450MHz (ISM)
    - ✓800-900MHz, 2.4GHz



- **Why 400MHz ?**
  - Lower path loss for low-power radio
  - 402-405MHz MICS implantable band
  - 420-450MHz band for wearable applications

Transceiver Design Challenges

1. **Low power**
   Radio dominates the node power



2. **Wide data rate range**
   From 10k (blood pressure)
   up to 3M (EEG streaming)

3. **Low cost**
   Same IC for HUB and node desired

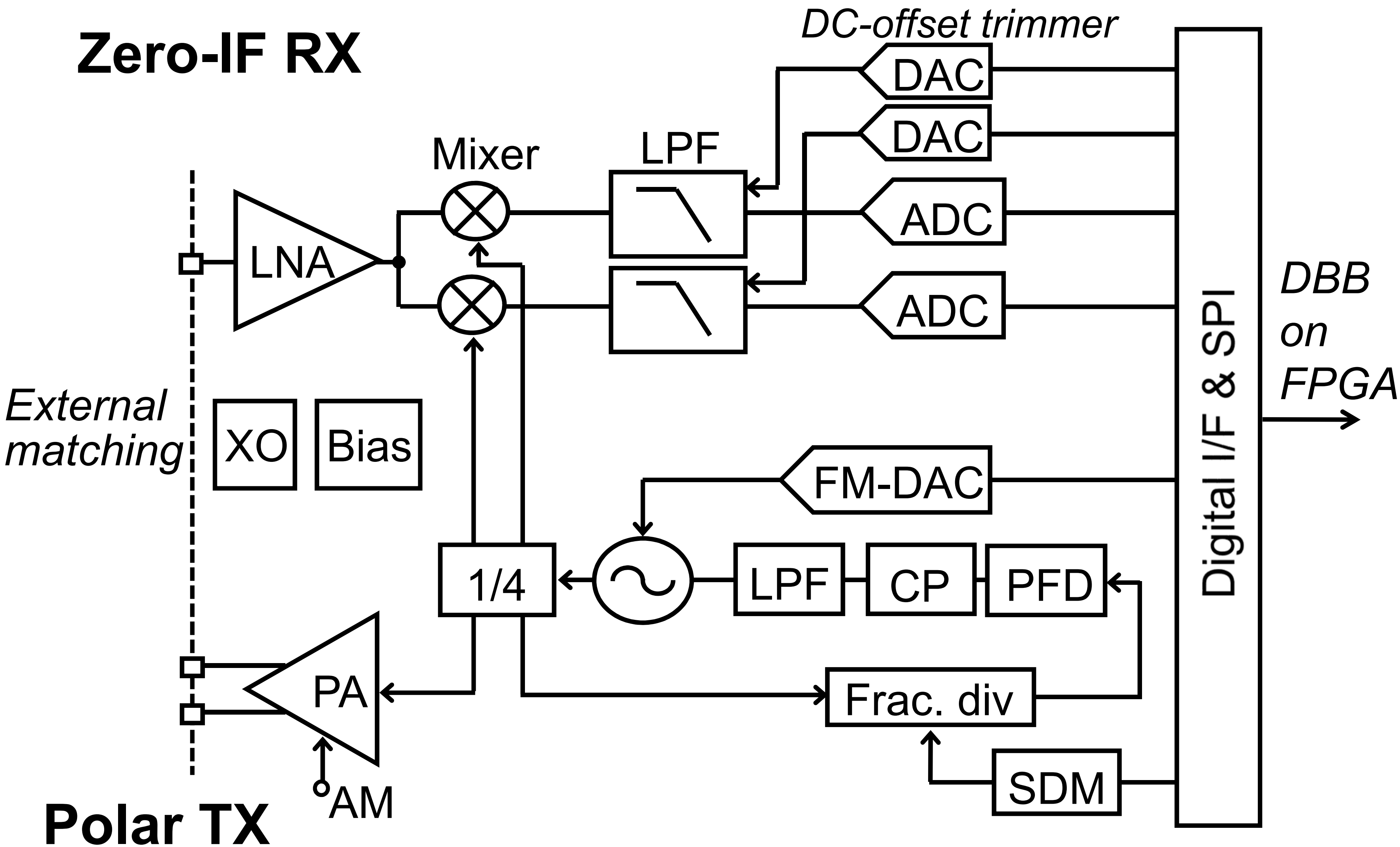
4. **Reliable communication**
   Path loss in/around body tighten link budget

Hans et al, "Radio Channel Characterization for 400 MHz Implanted Devices", WCNC 2014

Transceiver Target Specifications

Mode	15.6-compliant				Low Power (LP)	High Speed (HS)
Frequency [MHz]	402 - 405			420-450	402 - 450	
Modulation	π/2 DBPSK	π/4 DQPSK	π/8 D8PSK	GMSK	π/2 DBPSK	π/8 D8PSK
Data rate [kb/s] (w/o BCH coding)	187.5	375	562.5	187.5	11.7	4500
Spreading factor	1	1	1	1	16	1
RX sensitivity[dBm]	-92	-89	-83	-87	-95	-83
TX output power [dBm]	≤ -16			≥ -10	≤-16	≤-16

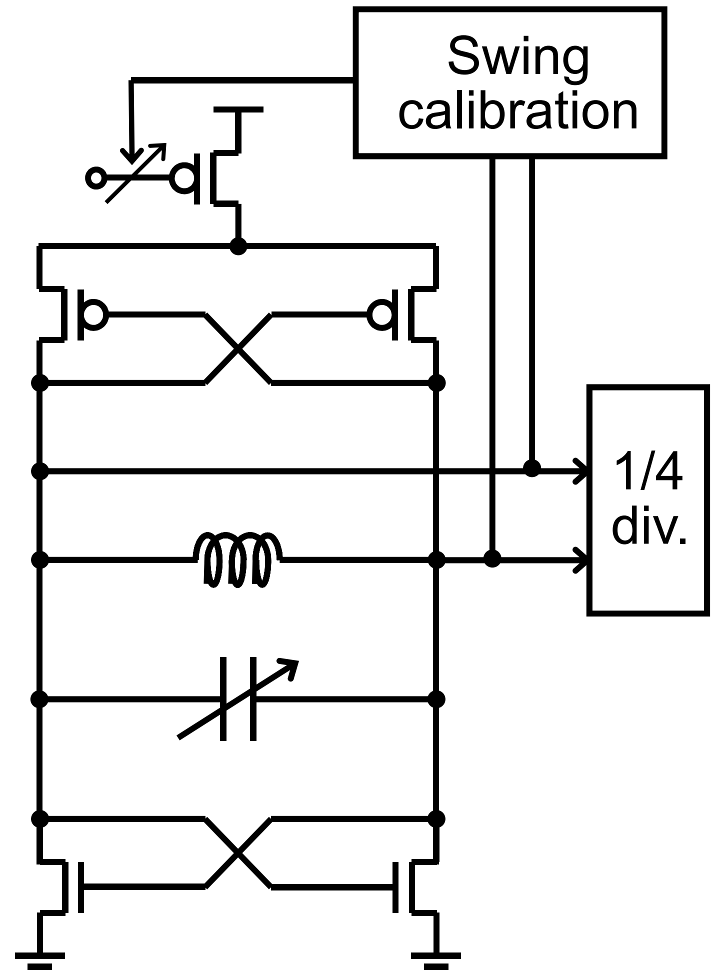
Transceiver Architecture



Low-Power VCO & Divider

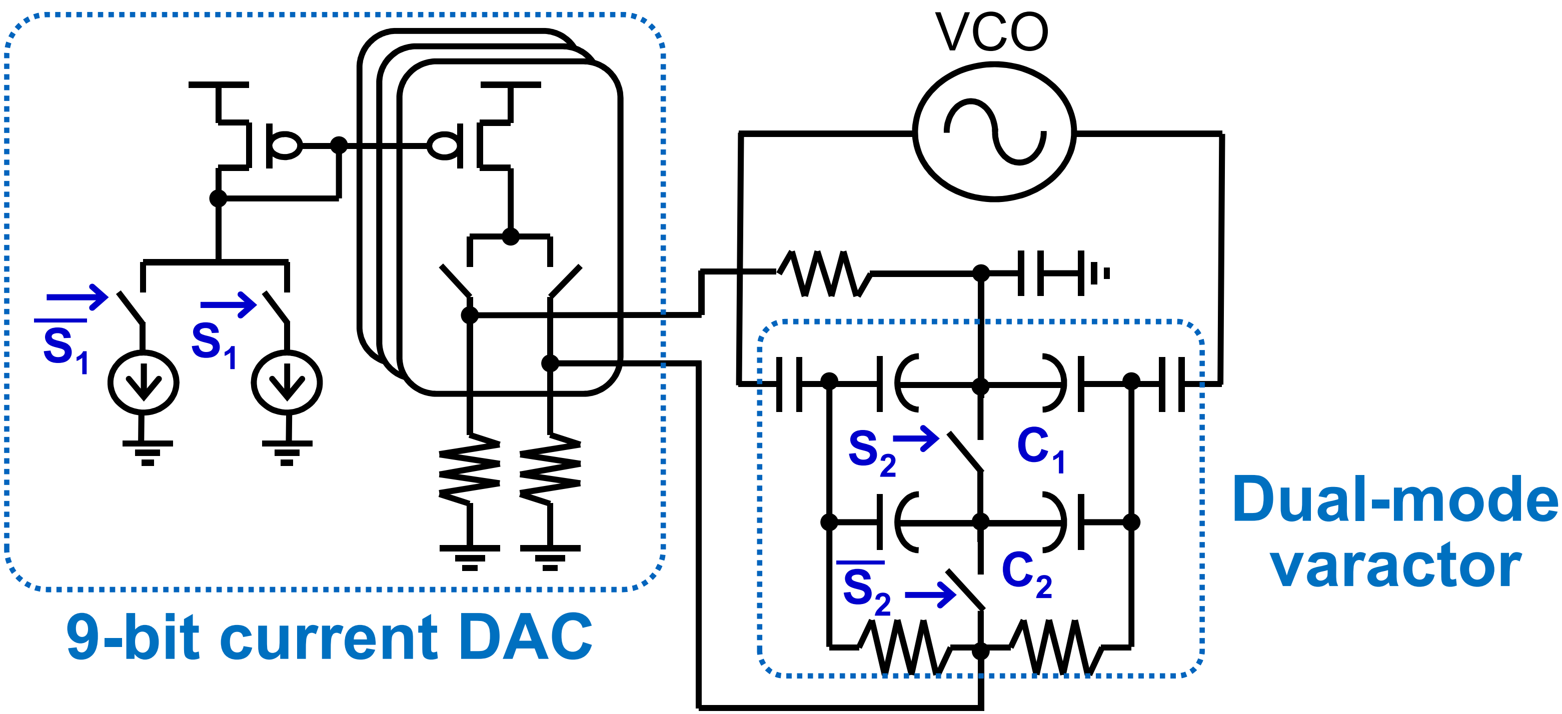
- 1.6GHz & 1/4 divider for optimal frequency planning:
  - P_{DC} of LC-VCO & divider have opposite dependency on frequency
- Low-swing 1/4 divider AC coupled to VCO:
  - 250mV_{DIFF} VCO swing required

  => no need for LO buffer
- VCO swing calibration loop:
  - optimize VCO P_{DC} & performances over PVT variations

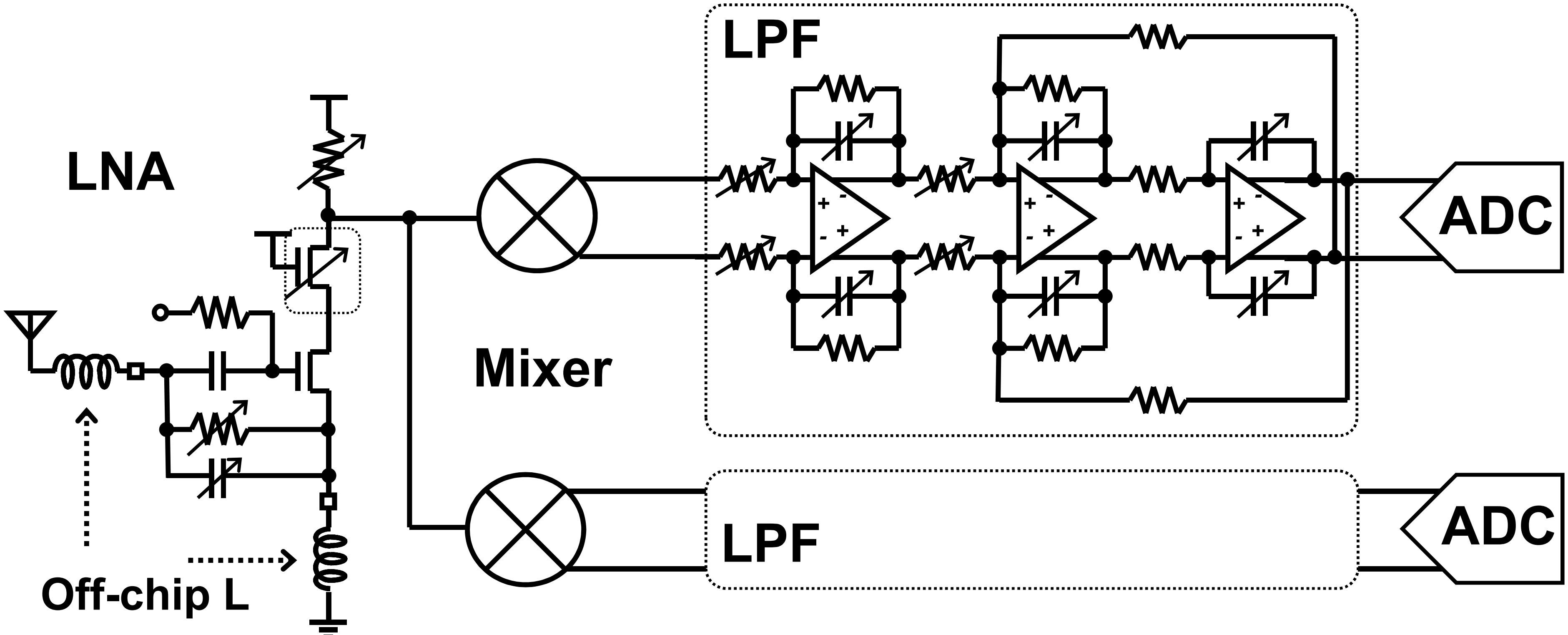


Wide-Range Frequency Modulation

Modulation	Data rate [kb/s]	FM range [kHz]	S1	S2	DAC bias current [μA]	C
GMSK	187.5	±50	0	0	0.4	C1
D8PSK	562.5	±800	1	0	4	C1
D8PSK (HS)	4500	±6000	1	1	4	C1+C2

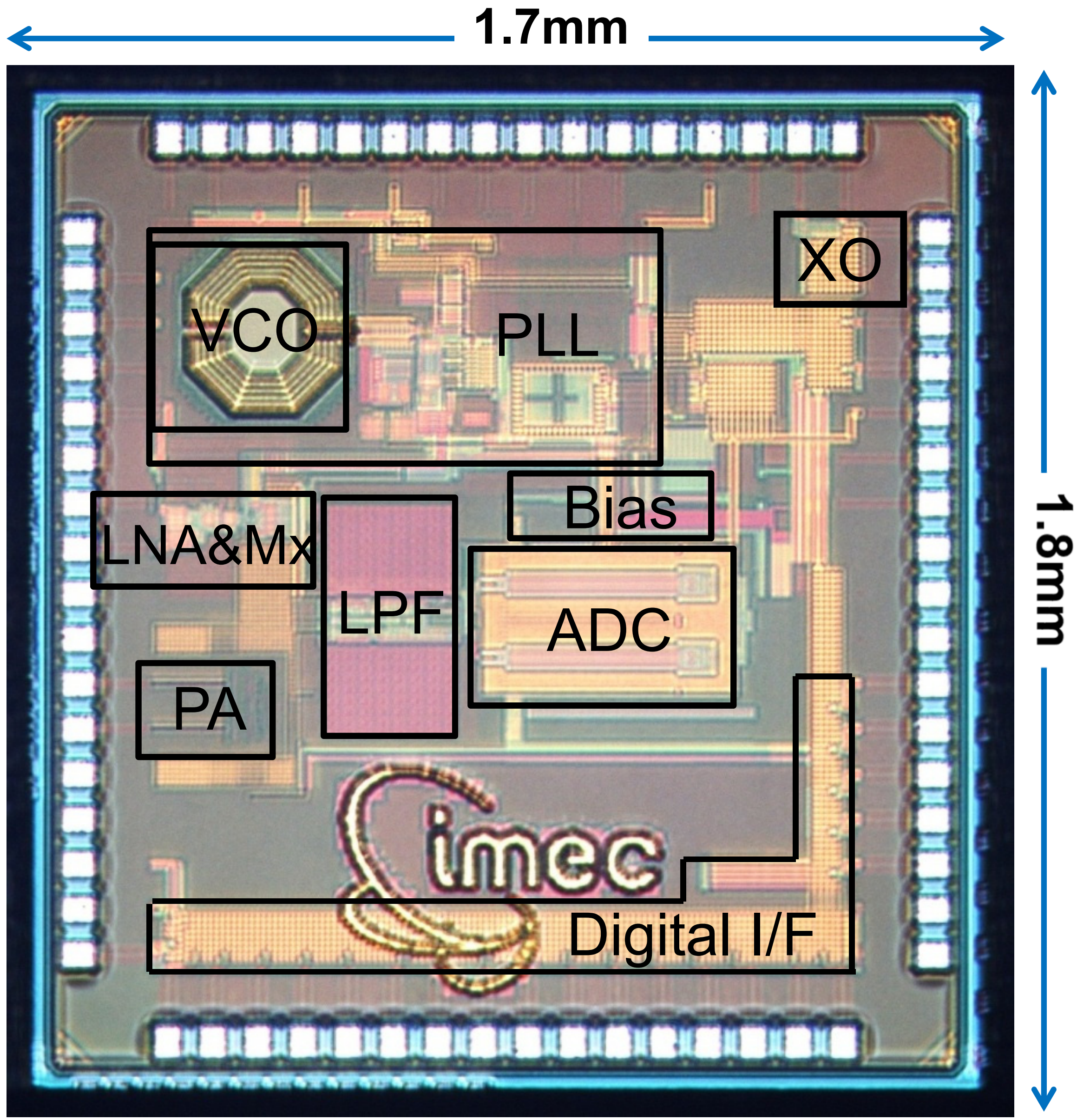


Re-configurable RX



Mode	15.6	LP	HS
LNA power consumption	400μW	100μW	400μW
LPF bandwidth	150kHz (MICS) 160kHz (ISM)		1.2MHz
ADC sampling rate	1.5MS/s		12MS/s

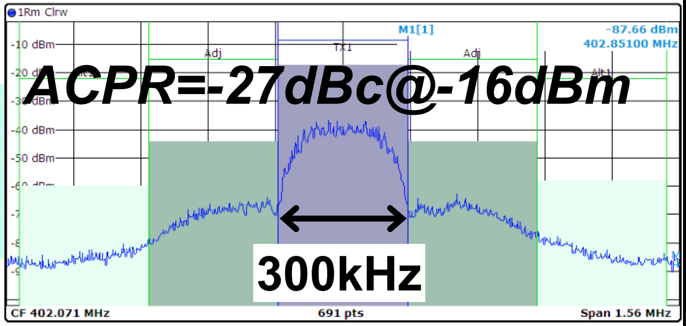
Chip Photo

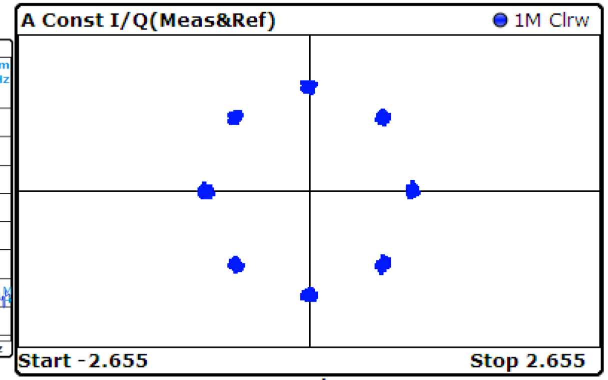


- Low-power 1-poly 8-metal 40nm CMOS
- 1V supply voltage
- Active chip area 1.02mm^2

TX Measurements

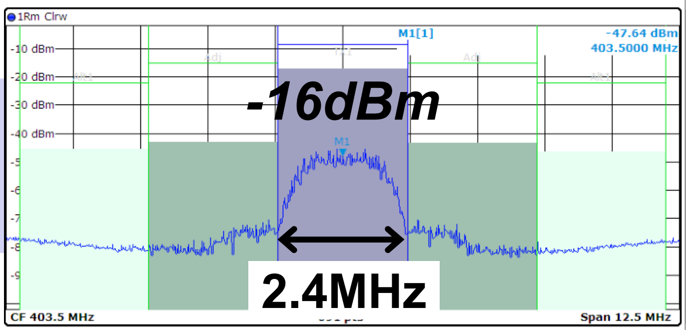
π/8 D8PSK
562.5kb/s

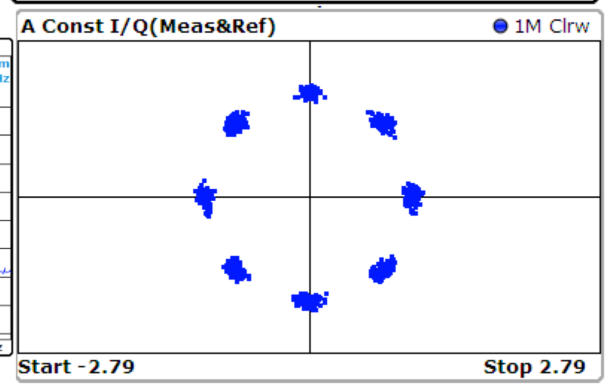




EVM=3.5%

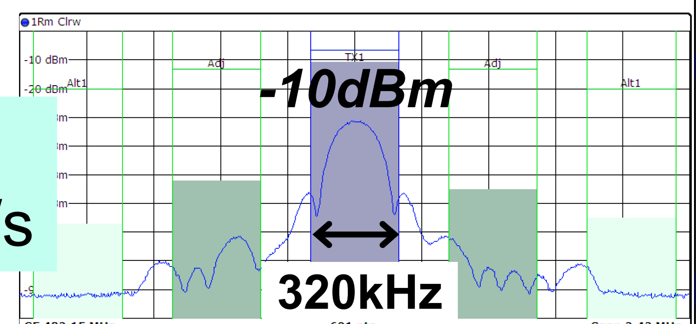
π/8 D8PSK
4.5Mb/s

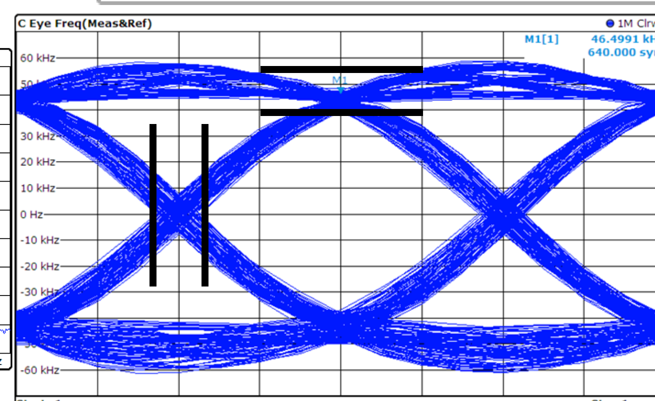




EVM=7%

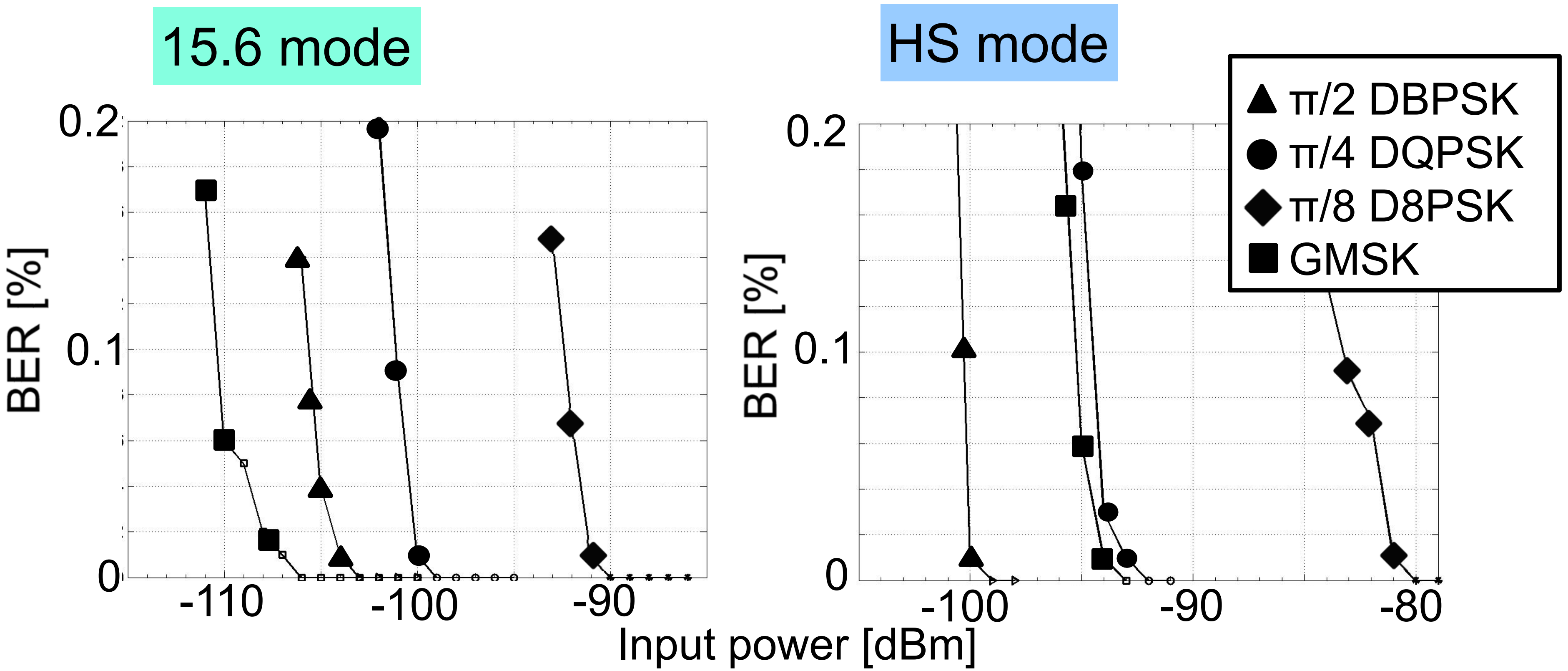
GMSK
187.5kb/s





Freq. error:
Upper
56.25 kHz
Lower
37.5 kHz

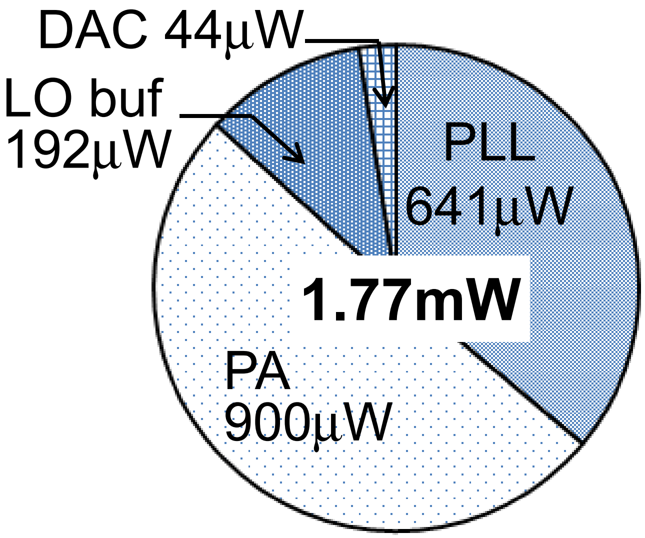
Sensitivity and ACR



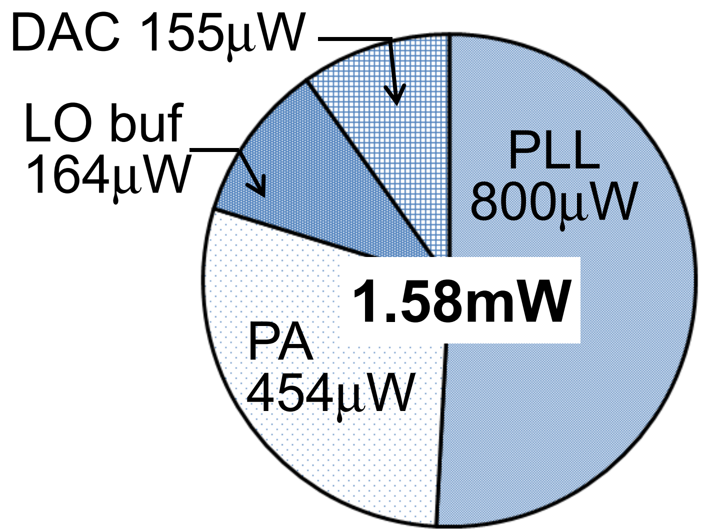
Modulation	Data rate [kb/s]	ACR [dB] @ 0.01% BER	
		Measurements	15.6 Specifications
π/2 DBPSK	187.5	15	14
π/4 DQPSK	375	14	10
π/8 D8PSK	562.5	8	5

Power Consumption

TX

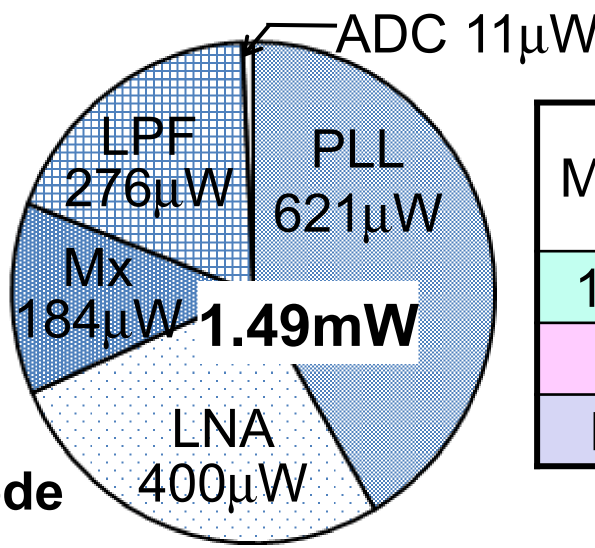


15.6, GMSK,P_{OUT}=-10dBm



15.6/HS, D8PSK,P_{OUT}=-16dBm

RX



15.6 mode

Mode	LNA [μW]	Mx&LPF&PLL [μW]	ADC [μW]	Total [mW]
15.6	400	1081	11	1.49
LP	100	1081	11	1.19
HS	400	1081	86	1.57

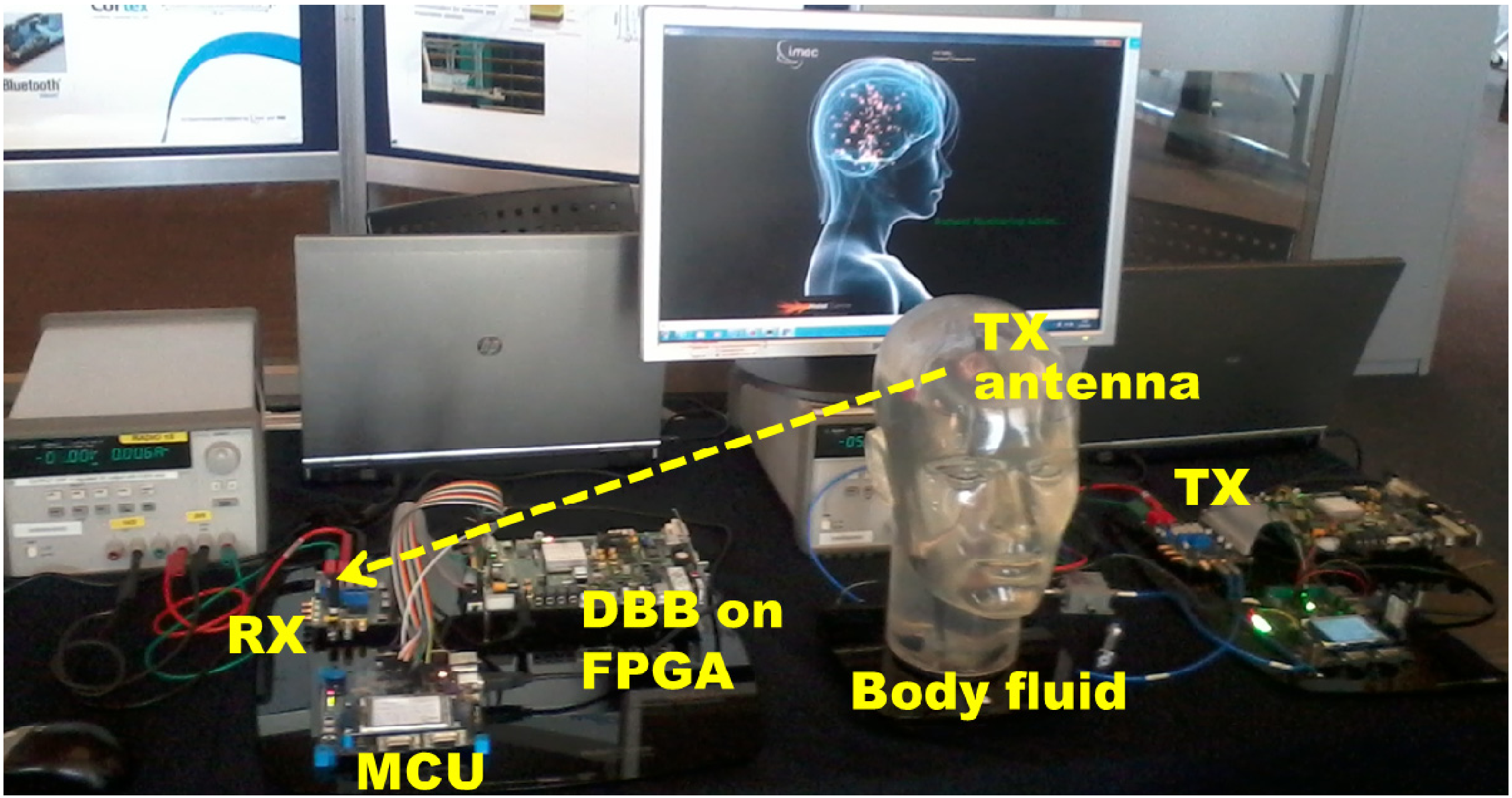
Performance Comparison

		AD ADF7021-V	Nordic nRF9E5	TI CC1101	B-CAS 06	ISSCC 05	This work		
Modulation		4-FSK MSK	GFSK	4-FSK OOK	FSK	FSK OOK	π/2 DBPSK	GMSK	π/8 D8PSK
DR[kb/s]		24	100	600	800	100	11	187.5	4500
Tech.		-	-	-	CMOS 0.18	CMOS 0.18	CMOS 0.04		
TX	**P_{DC} [mW]**	31	21	23	11	27	2.28 (*2)	2.27 (*2)	2.28 (*2)
	Pout [dBm]	0	-10	-6	-4.5	10	-17	-10	-17
RX	**P_{DC} [mW]**	42	23	30	11	2.1	1.9(*2)	2.2 (*2)	2.2 (*2)
	Psens [dBm]	-114	-100	-95	-83(*1)	-111	-112	-110	-83

(*1) Sensitivity in dBm calculated with 90uV & 1.6kΩ
(*2) Simulated DBB power of 0.5mW(TX) & 0.7mW(RX) added to the measured AFE

400MHz Transceiver Demo

- Low-power AFE transceiver, DBB on FPGA & MCU



Conclusions

- 400MHz medical transceiver for implant and wearable applications in 40nm CMOS
- Re-configurable for sensor node and HUB devices
  - IEEE802.15.6 compliant mode
  - 11kb/s low-power control mode
  - 4.5Mb/s high-speed mode for streaming applications
- Best-in-class low power consumption
  - 1.6mW RX and 1.8mW TX both @ 1V
- State of the art performances

An 860μW 2.1–2.7GHz All-digital PLL-based Frequency Modulator with a DTC-assisted Snapshot TDC for WPAN (Bluetooth Smart and ZigBee) Applications

V.K. Chillara[12*], Y.H. Liu[1], B.Wang[12], Ao Ba[1], M.Vidojkovic[1], K. Philips[1], H. de Groot[1],R. B. Staszewski[2]

[1]IMEC-Holst Centre, Eindhoven, The Netherlands

[2]Delft University of Technology, Delft, The Netherlands

***now at Analog Devices, Limerick, Ireland**

TU Delft Delft University of Technology

Holst Centre Open Innovation by IMEC and TNO

imec

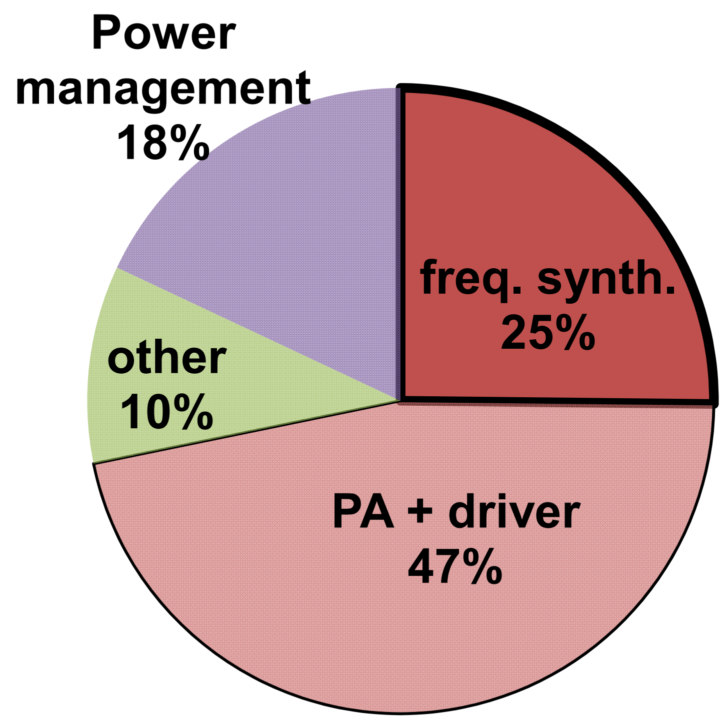
Outline

- Introduction
- Low-power ADPLL techniques
- Circuit Implementation
- Measurement Results
- Conclusion

Why Ultra Low Power ADPLL?

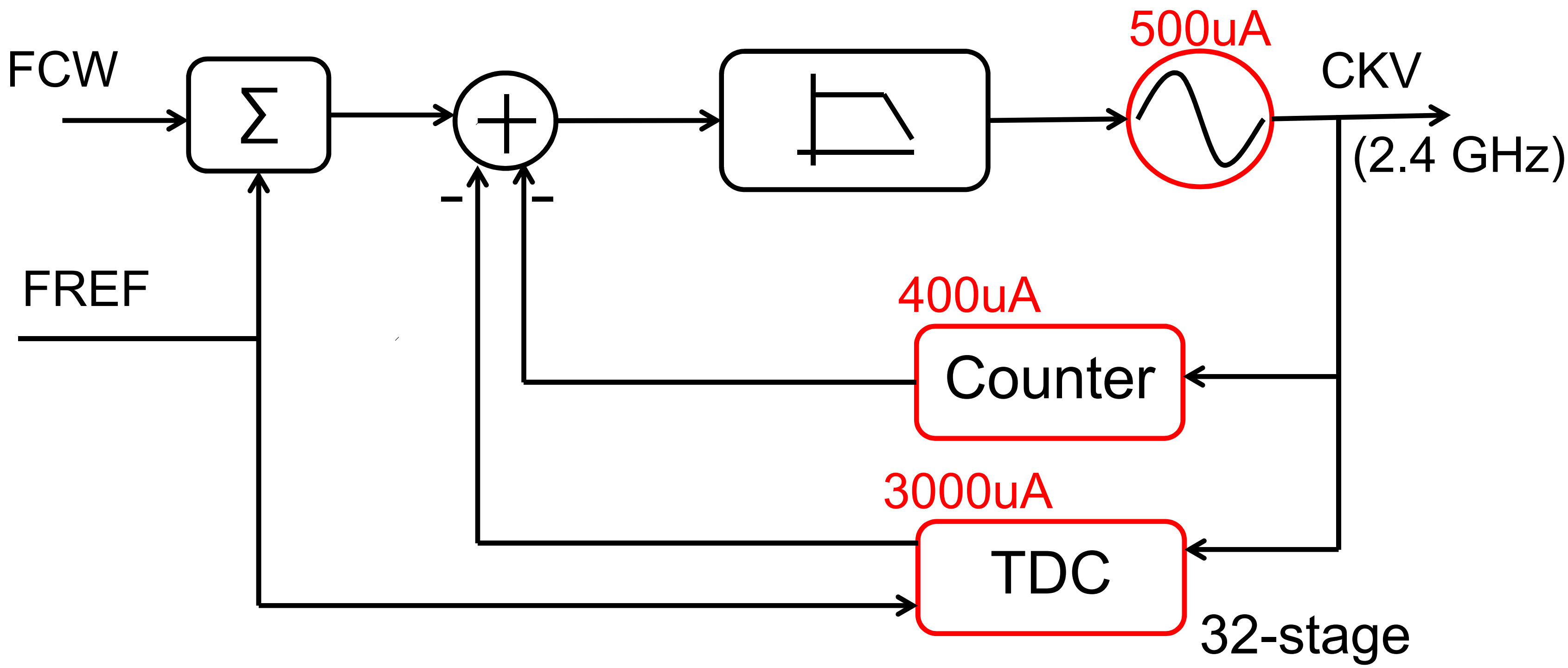
- Autonomous operation is key to WSN nodes
- Frequency synthesizer consumes about 25 – 30% [1]
- Sub-mW PLL key to realize energy autonomy
- ADPLLs are better suited in nanoscale CMOS

WSN Power



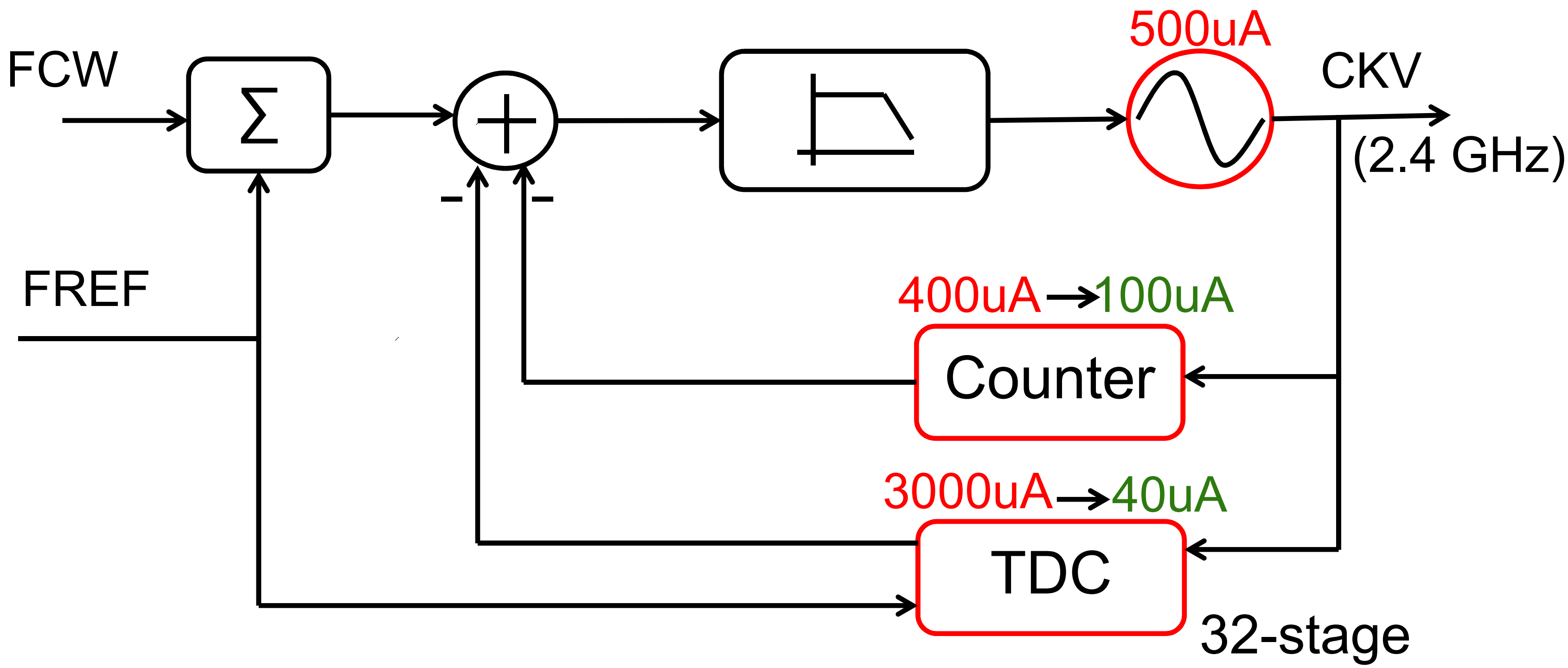
[1] Y.H. Liu, ISSCC'13

Counter-based ADPLL



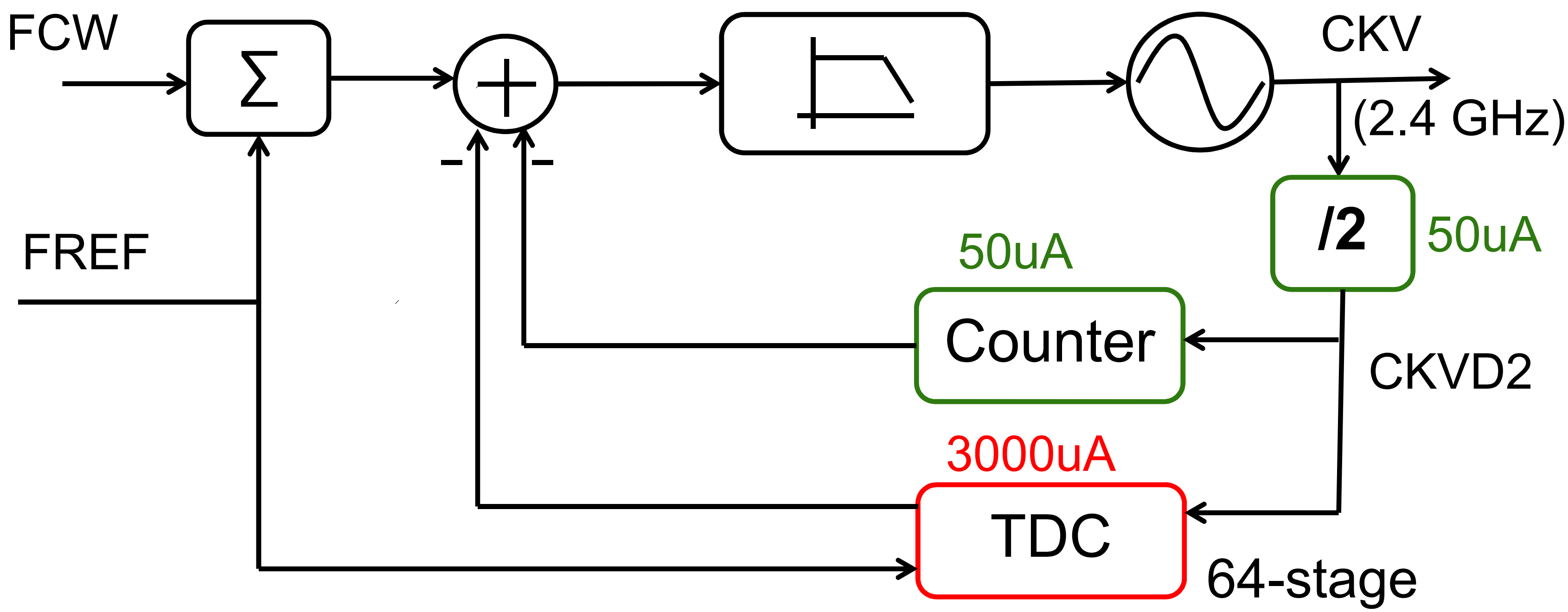
TDC needs a large operating range and runs at high CKV frequency → power hungry

Counter-based ADPLL



TDC needs a large operating range and runs at high CKV frequency → power hungry

ADPLL – Low Power Techniques



Frequency division enables the use of asynchronous counter → reduced power consumption

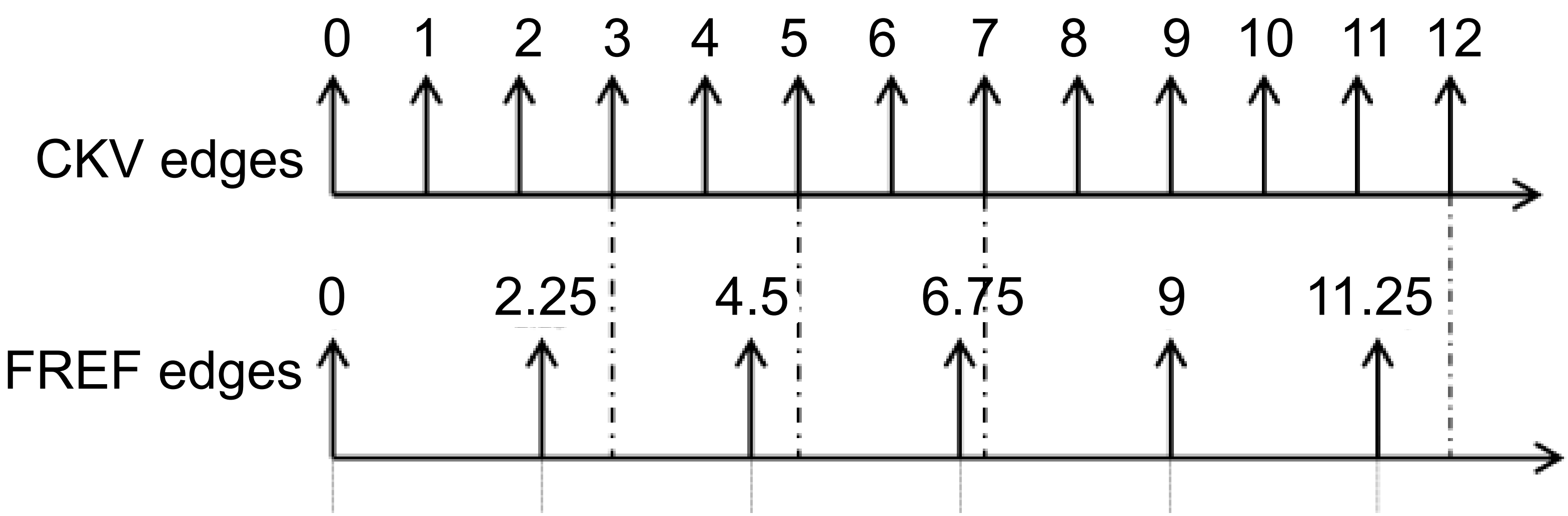
ADPLL – Low Power Techniques

Lowering TDC range

Align FREF and CKV before feeding to TDC

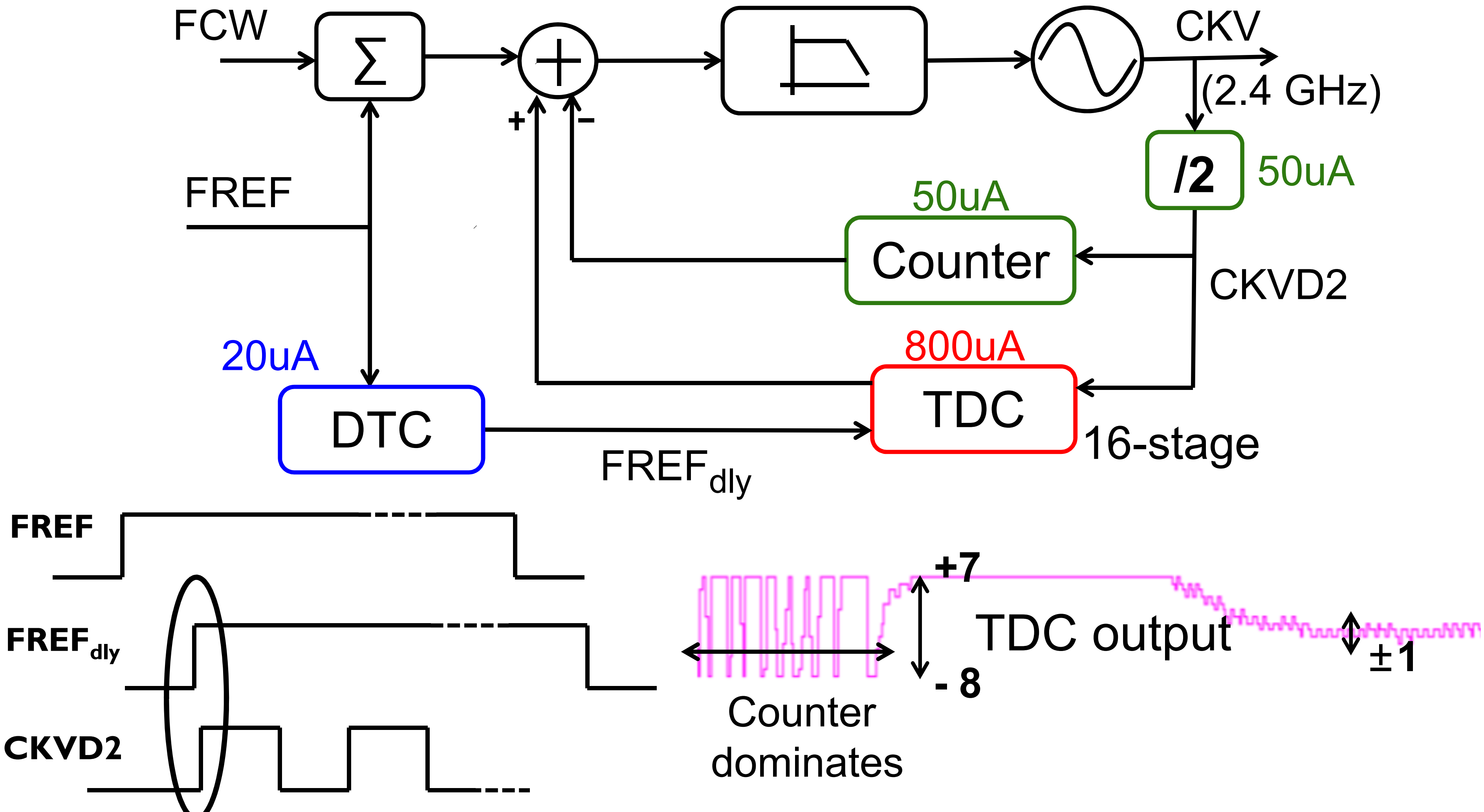
Accumulated fractional part of FCW is used

For FCW = 2.25,



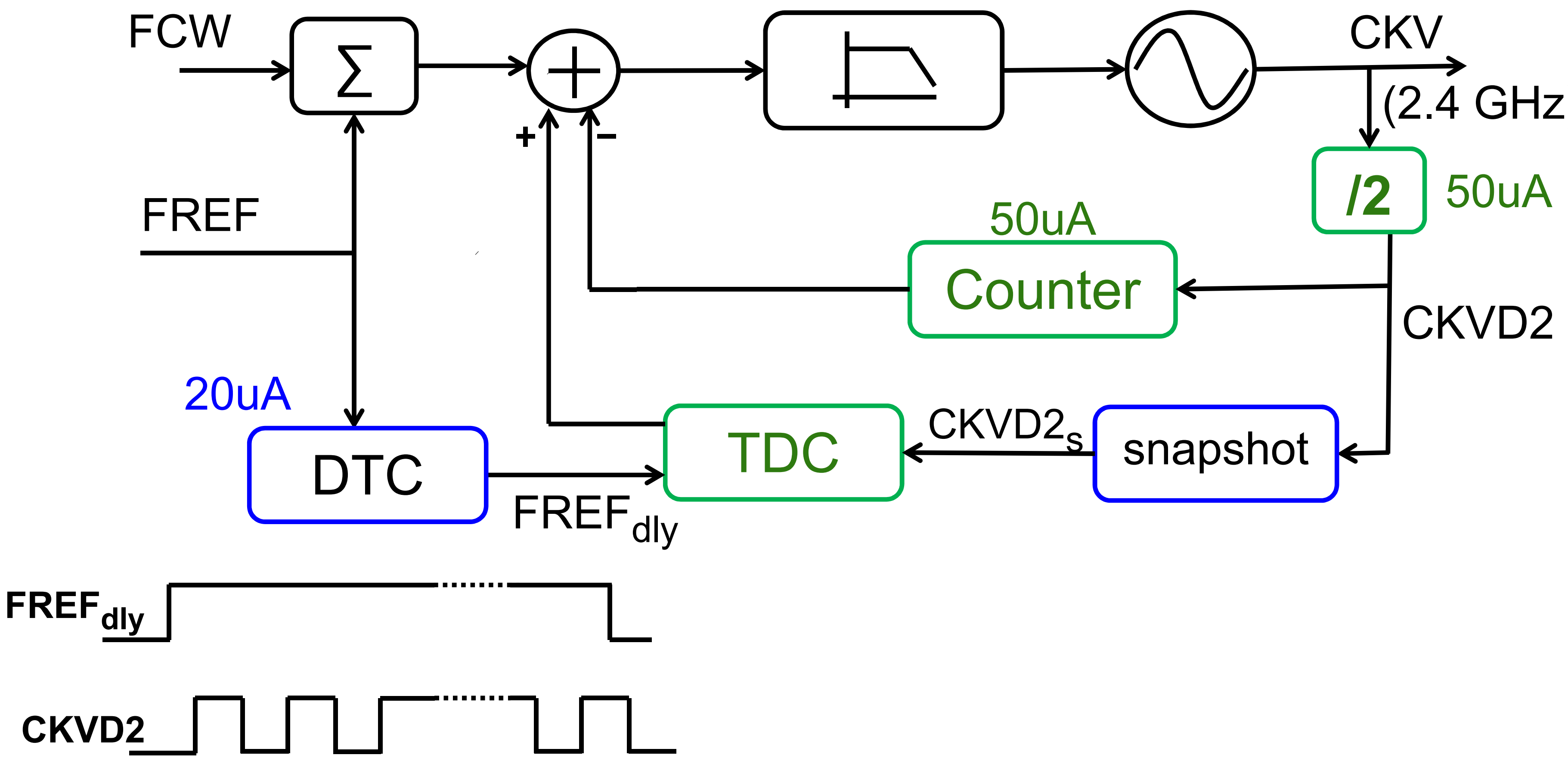
ADPLL – Low Power Techniques

Lowering TDC range



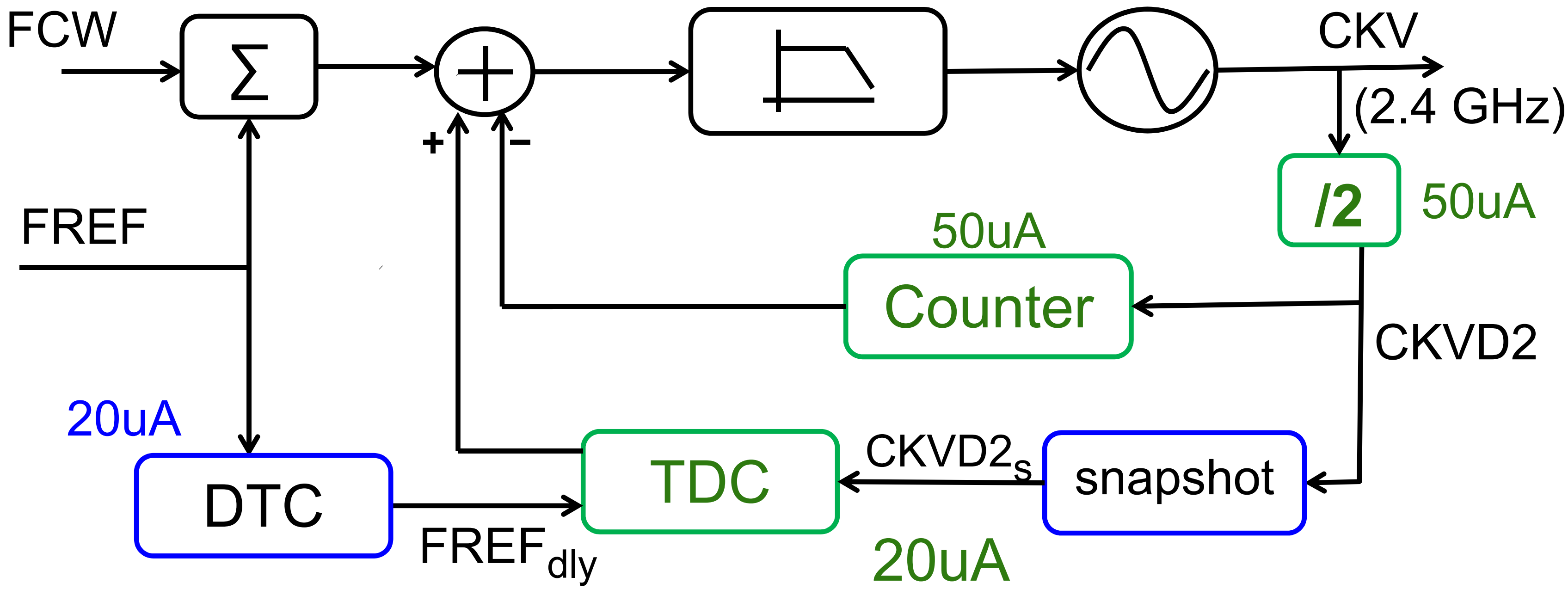
ADPLL – Low Power Techniques

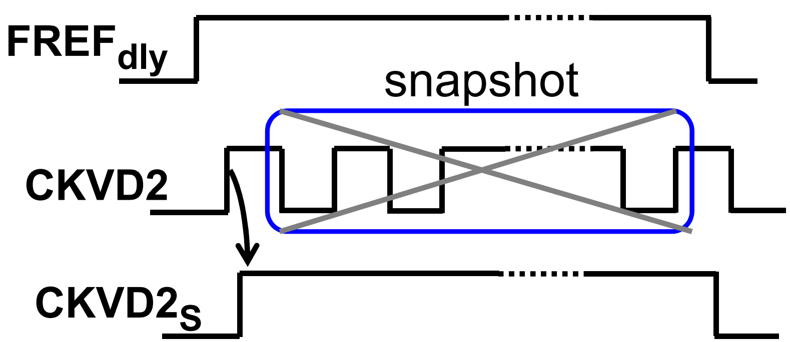
Reducing operating frequency



ADPLL – Low Power Techniques

Reducing operating frequency





TDC frequency reduced from CKVD2 → FREF (~40x in this work)

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  - DTC-assisted snapshot TDC
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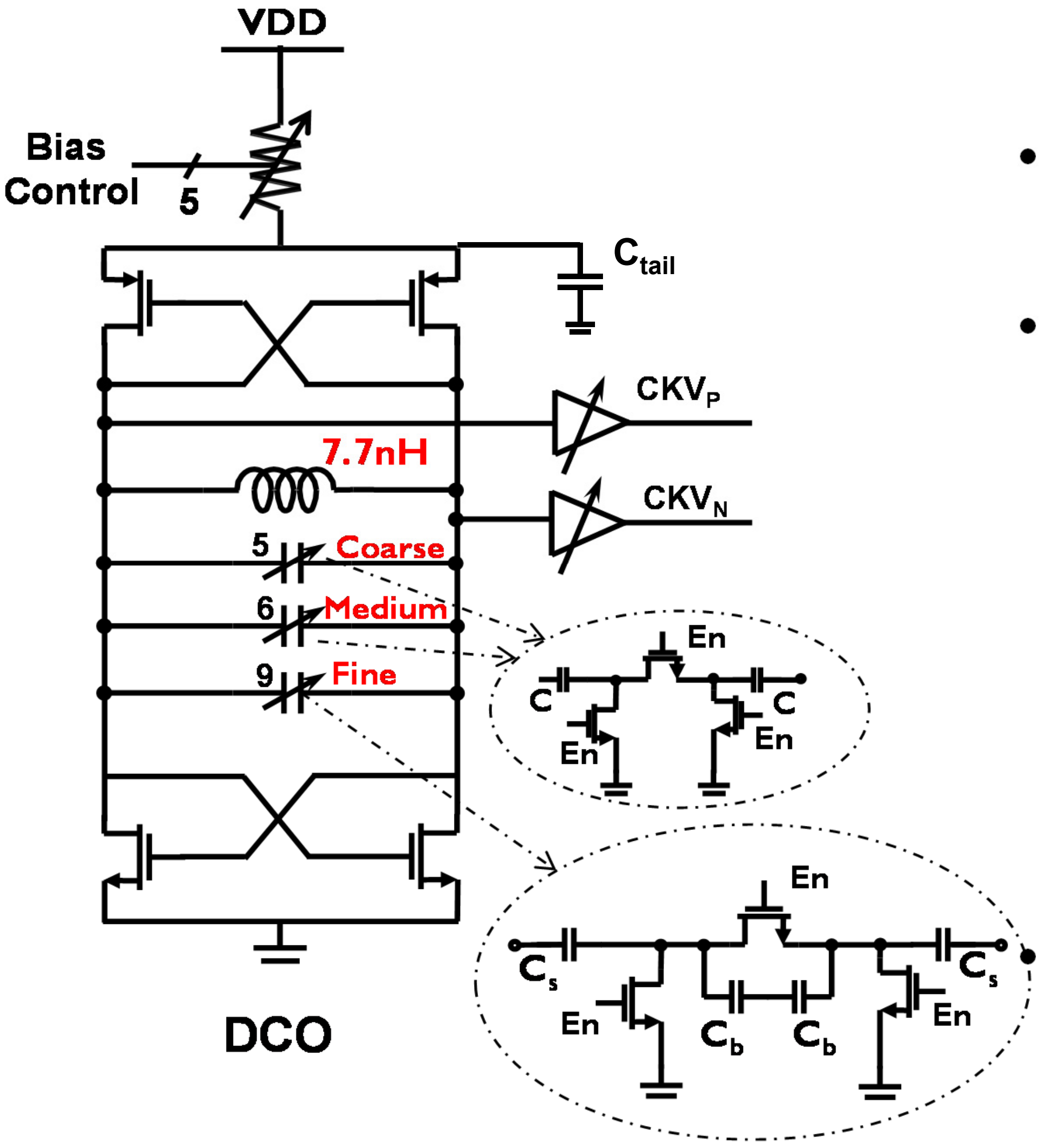
2.1–2.7GHz DCO



- MOM caps are less sensitive to VT variation
- The resolution of the fine bank:

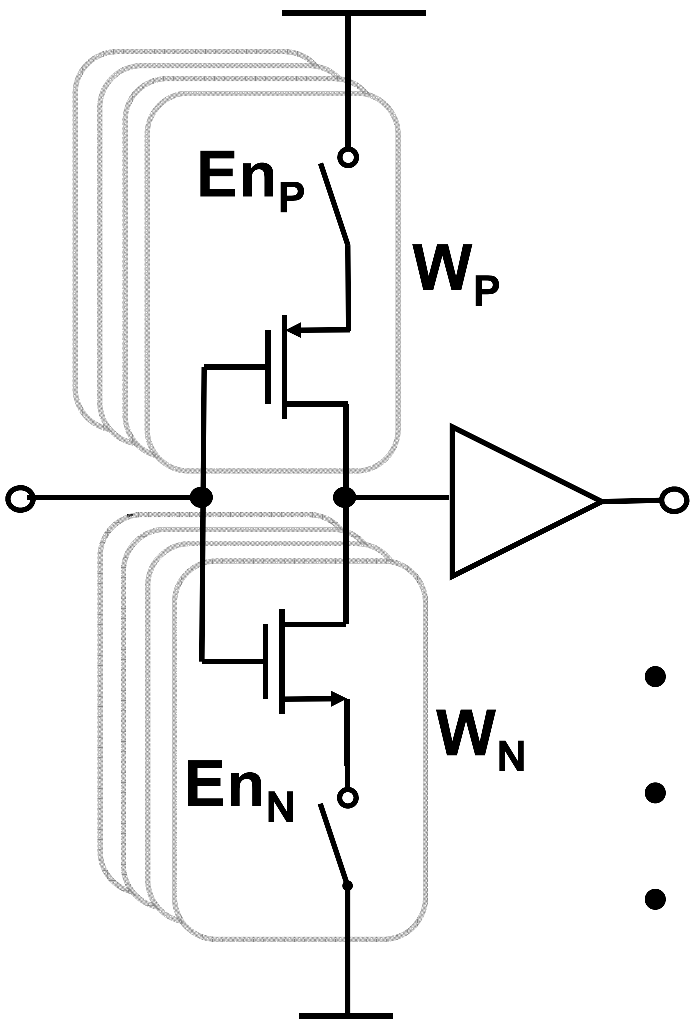
$$C_{max} = Cs/2$$
$$C_{min} = CsCb/(2(Cs + Cb))$$
$$\Delta C \approx Cs^2/(2Cb)$$

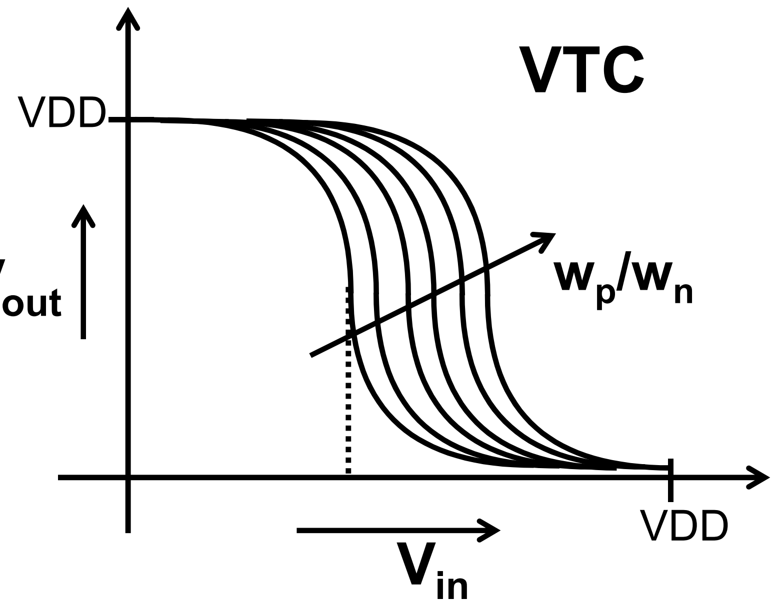
Cb >>> Cs

18 aF

- Effect of parasitics and mismatches is reduced

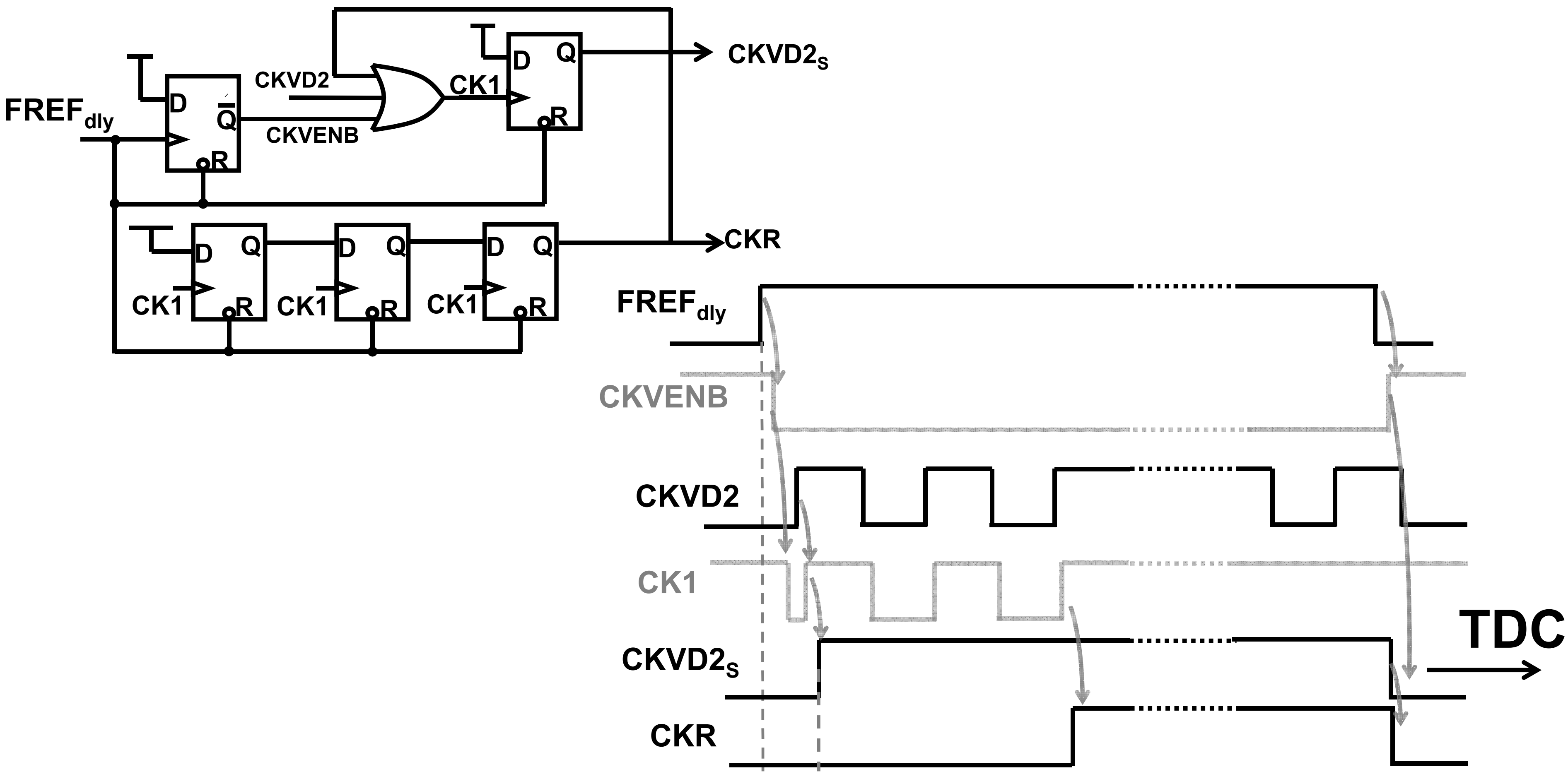
DC-coupled DCO Buffer





- Avoids driving bulky decoupling cap.
- The VTC is varied by controlling Wp/Wn
- Output DC-level is calibrated automatically across PVT

Snapshot Circuit



FREF$_{dly}$ triggers the snapshot to catch the first CKVD2 edge in every reference cycle

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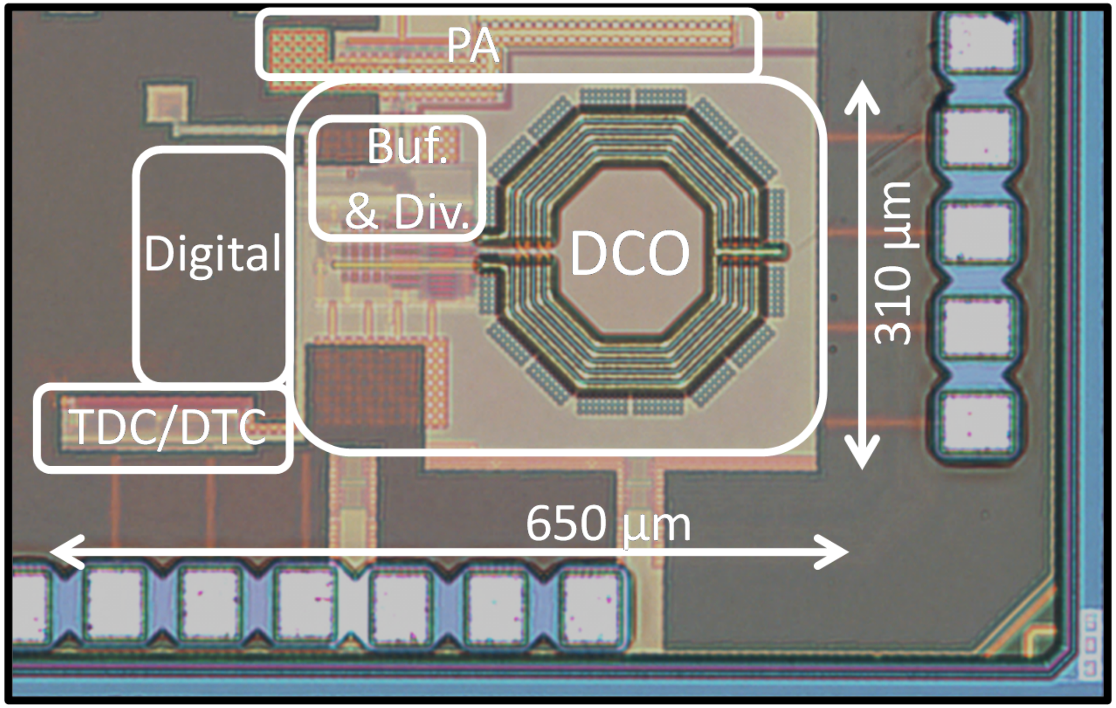
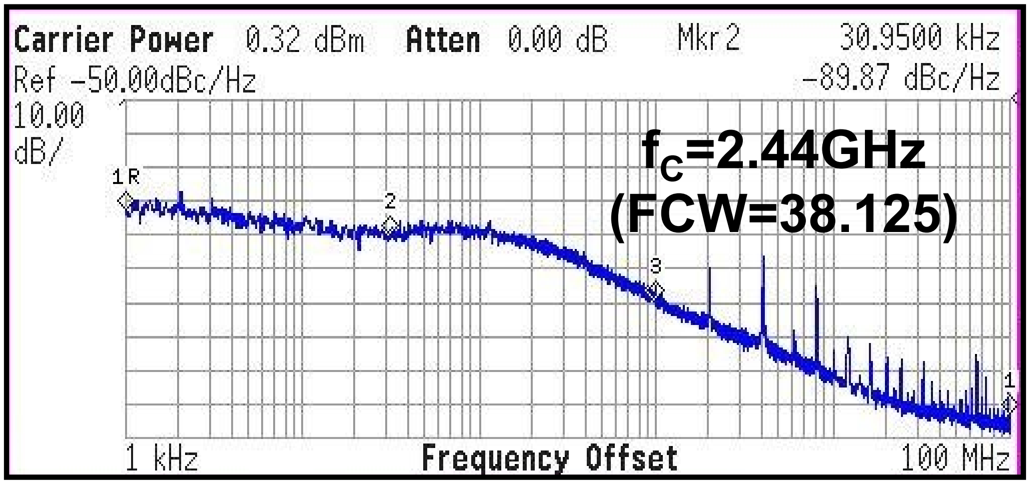
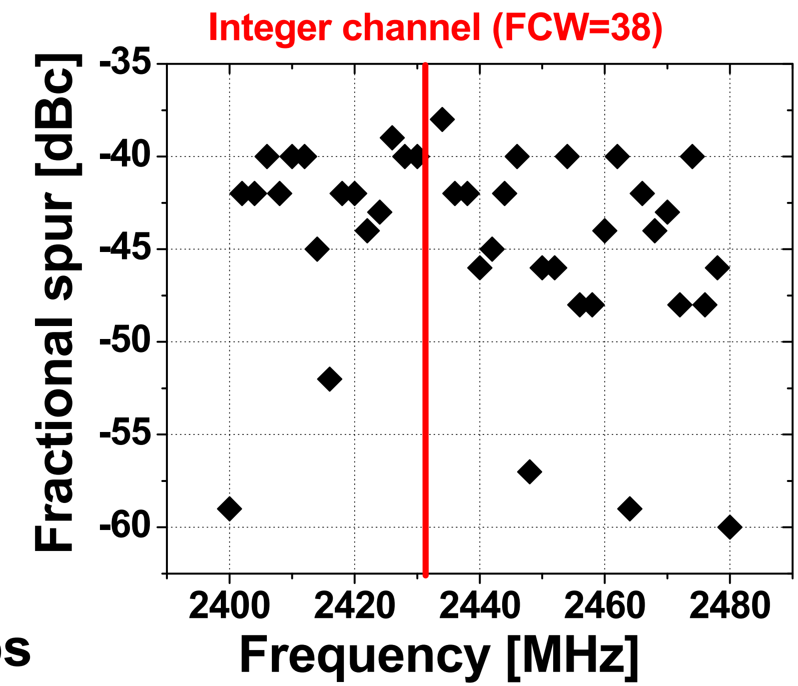
Chip Photo



- Implemented in TSMC 40nm 1P8M LP CMOS
- Occupies a core active area of 0.2 mm^2

Phase Noise and spurs



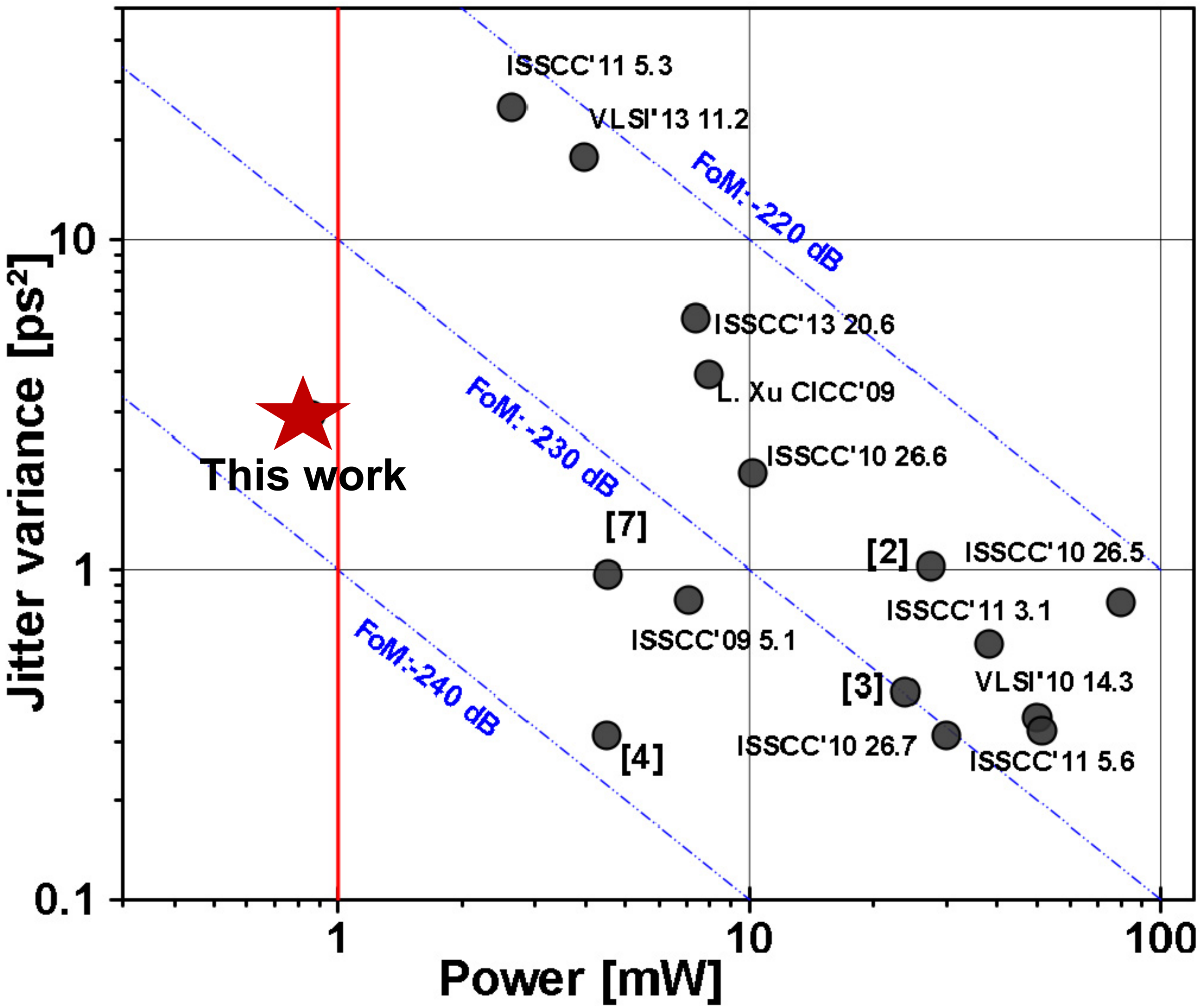


-90 dBc/Hz @ 30kHz
-109dBc/Hz @ 1MHz

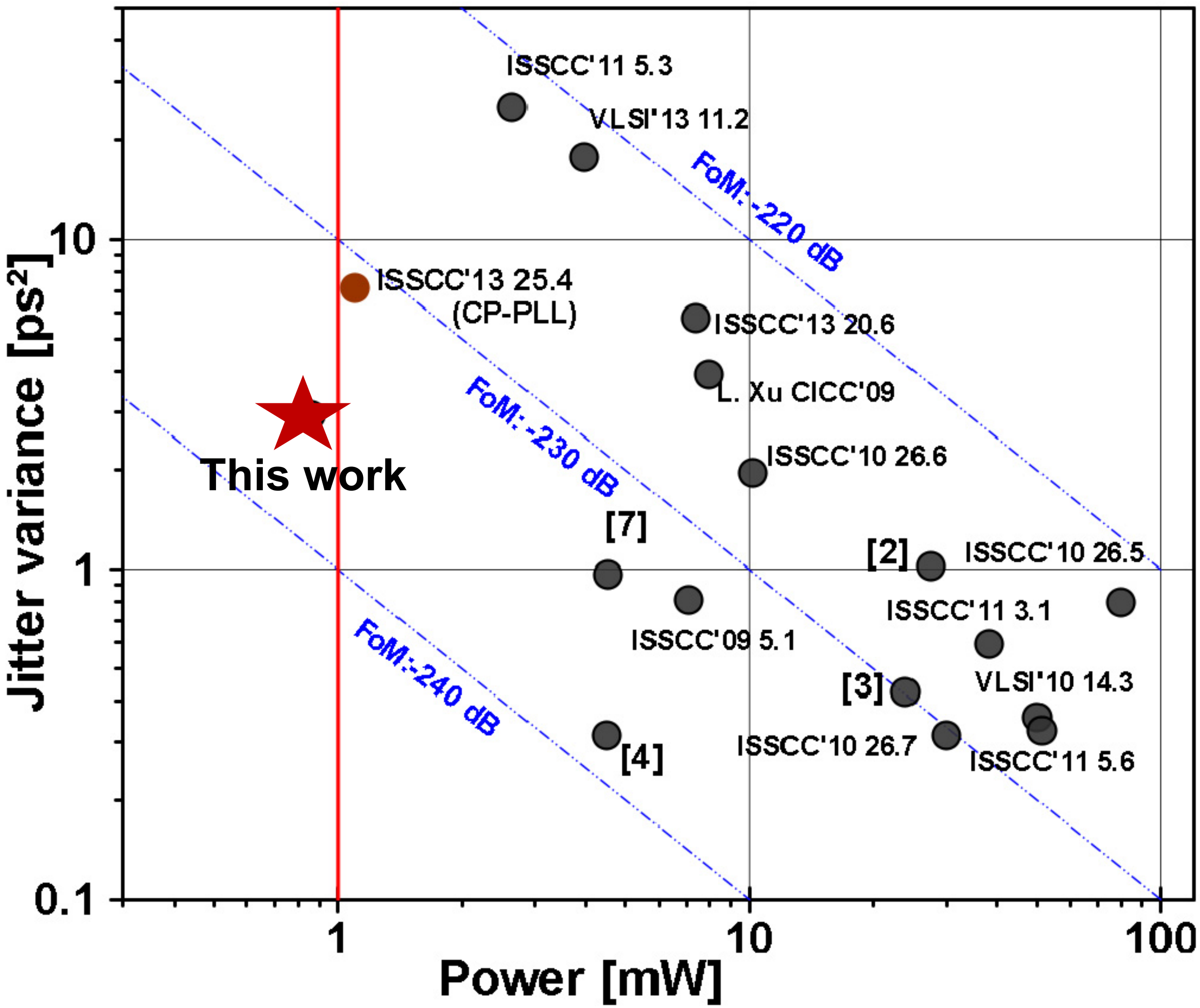
RMS jitter = 1.71ps

- Worst case fractional spur across Bluetooth Smart channels is -38dBc (spec.: <-30dBc)
- Consumes 860 μW at 1V supply

Benchmark with other ADPLLs



Benchmark with other ADPLLs



Conclusion

- Several low-power techniques are demonstrated
  - Edge prediction with DTC
  - Snapshotting TDC
  - DC-coupled DCO buffer

- Consumes 860 μW with 1.7ps rms jitter and -236 dB FoM

- The first-ever wireless (AD)PLL to break the 1mW barrier, while complying with the BL-Smart and ZigBee standards